A Programmable 7GHz Frequency Divider in a SiGe Bipolar Technology for Highly Linear Fractional-N Ramp Generation

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I. INTRODUCTION

Millimeter wave radar systems are well suited for applications in automotive and industrial distance measurement sensors. The precision of FMCW radar systems notably depends on the bandwidth and the linearity of the generated frequency ramps.

Thus, high precision and high speed measurement systems are in need of highly linear frequency ramps. The realization requires a phase-locked loop (PLL) with an adjustable output frequency as shown in figure 1. Compared to other concepts of generating frequency ramps, the PLL offers the most stable performance in the millimeter wave region.

The PLL's output frequency is determined by the division ratio of a frequency divider in the loop. Distinct improvement in linearity and noise is achieved by fractional synthesizers. These require high speed programmable dividers and fast switching of the division ration in a wide range [1]. Higher output frequencies are achieved by adding a prescaler, mixer or multiplier in the system. For the best noise performance the system should be designed for low division ratios and thus a high reference frequency.
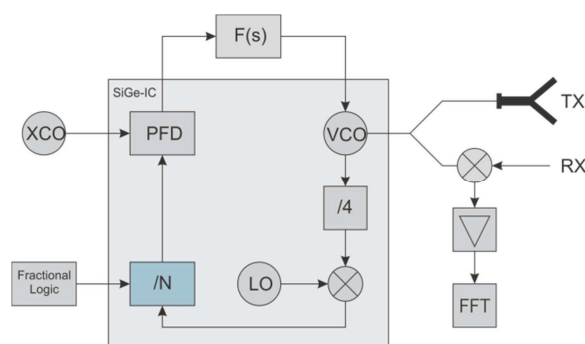

Figure 1: Block diagram of a fractional-N phase locked loop for an intended application in a FMCW radar system
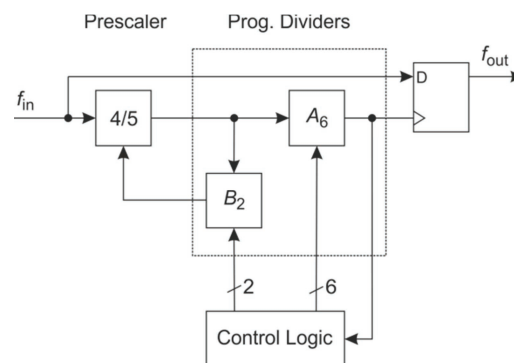

Figure 2: Block diagram of the dual-modulus divider using a divide-by-four/five prescaler and two programmable dividers

In this paper, a dual-modulus prescaler and a programmable divider for input frequencies up to 7 GHz is presented. The presented circuit is implemented in Infineon's 0.35 µm high frequency SiGe bipolar technology (f_T=200 GHz, f_{max}=250 GHz) and uses completely differential current mode logic, which serves for high speed and high reliability.

A further advantage of using a high speed bipolar technology is the possibility to integrate millimeter-wave components such as a voltage controlled oscillator (VCO) on the same chip as illustrated in figure 1. For instance, in [2] a VCO at 80 GHz Center Frequency was implemented in the same SiGe bipolar technology. Although millimeter wave VCOs have been realized in CMOS technologies [3], the performance and in particular the wide tuning range apparently cannot be achieved.

For the presented phase-locked loop a frequency divider operating up to 7 GHz input frequency is well suited. Being implemented in the same technology the frequency divider, presented in this paper, can be integrated on the same chip as the VCO.

The complete circuit gives a cost, area and power efficient solution for usage in high speed phase-locked-loops for e.g. millimeter-wave FMCW radar systems. Beyond that, fractional ramps with high linearity and stability are essential for other applications like e.g. fast network analyzers.
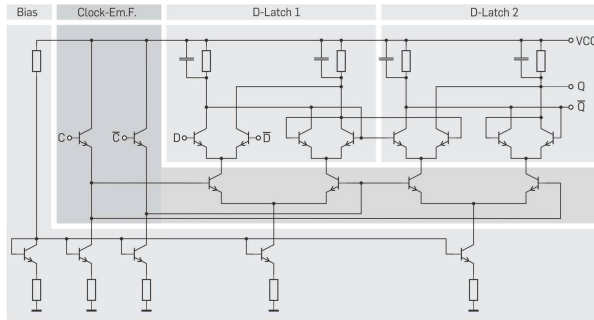
Figure 3: D-FF in Current-Mode-Logic (CML). Capicators represent parasitic internal wire-capacitances.
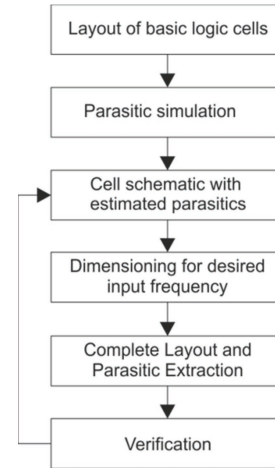

Figure 4: Design flow for power optimization of the implemented circuit

II. ARCHITECTURE

Figure 2 shows the block diagram of the dual-modulus divider. The divider uses a synchronous prescaler with a division ratio which can be set to four or five as input stage [4]. The prescaler is followed by a more complex logic circuit consisting of two frequency dividers with programmable division ratios.

Thus, while the prescaler is designed for high input frequencies, the latter is optimized for low power consumption due to its lower operating frequency. On the one hand a higher tail current and prescaler division ratio would allow higher input frequencies, but on the other hand the divider's minimum division ratio is determined by the prescaler. For the best noise performance the system should be designed for low division ratios and thus a high reference frequency.

For minimum jitter of the output signal and optimum phase noise the output pulse of divider A and the input signal are synchronized to the input frequency by an output D-flip-flop with high tail-current. The division ratio f_{in}/f_{out} ranges from 12 to 255 and can be set via an 8 bit parallel interface for high programming frequencies above 100 MHz. The divider output stages are directly driving a phase-frequency detector.

The prescaler's division ratio is modulated by the output of the 2 bit divider stage B. As long as B's output is LOW the prescaler divides by 5 (B clock cycles). When reaching the target value B's output becomes HIGH and the prescaler divides by 4 for the rest of the (A-B) clock cycles.

$$T_{out} = T_{in} \cdot \left(5 \cdot B + 4 \cdot (A - B) \right)$$

The overflow of divider A resets the circuit and enables the control logic to set a new division ratio. Thus, the combination of all blocks according to figure 2 leads to an output frequency:

$$f_{out} = \frac{f_{in}}{4A + B}$$

Here, A and B are the division ratios of both programmable dividers. To set every division ratio between 12 and 255, divider A uses 6 Bit and divider B 2 Bit.

The block diagram of divider A is shown in figure 5. Each highlighted block divides the input signal by 2 using a feed back D-flip-flop and two logic gates for linking it with the output of the previous stages. The divider counts up until A and Q match. The following output pulse resets both counters A and B und thus starts a new clock cycle. For division ratios of higher or lower bit width the highlighted block is adequately duplicated. Due to the modular architecture of this and all other circuit stages, the divider can easily be adapted and extended and even the full radar system including the fractional divider logic can be implemented on one chip. The parallel control logic interface enables the divider to use different division ratios in each output clock cycle and thus generating highly dynamic fractional frequency ramps.
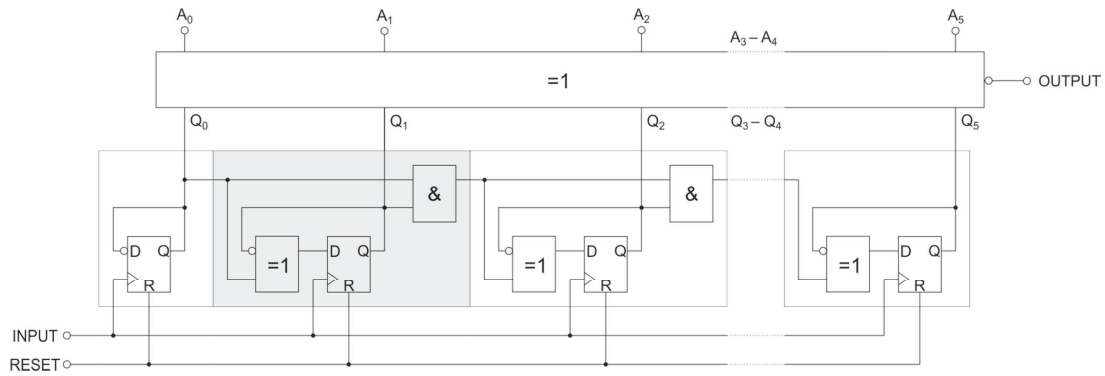
Figure 5: Synchronous Divider A counts up until A and Q match. Each D-flip-flop stage divides the input frequency by 2. In the dual-modulus concept divider A's OUTPUT pulse enables the RESET signal. The divider is designed for 6 Bit (A<64). For higher division ratios N, the highlighted block can be duplicated adequatly.

III. DESIGN FLOW AND SIMULATION

To optimize the circuit for the right proportioning between power and speed, apart from the simulation models of the used bipolar transistors, parasitic capacitances induced by the layout have to be taken into account.

Thus the circuit is iteratively dimensioned. Figure 4 shows the design flow schematically. Firstly, basic logic gates are layouted and parasitic capacitances are extracted. The capacitances, parallel to the load resistors as shown in figure 3 are estimated by simulating the step response of these gates, then reproduced in the schematic of each cell. These capacitors represent the transistor and internal wiring capacitances. By parametric sweeps of the tail current of each cell, the circuit is optimized for the desired input frequency. Due to additional wiring capacitances and other parasitics, the circuit is resimulated after implementation and parasitic extraction of the complete layout to verifiy operation in the entire division ratio and frequency range. For some parts of the circuit minor adaption is necessary or buffers need to be added after stages with high load capacitance.

IV. MEASUREMENT RESULTS

A chip photograph is shown in figure 6. The total chip area taken by the frequency divider is 0,15 mm². The divider operates with a supply voltage of 3.3 V at a total power consumption of 130 mW including output drivers and the 8 bit logic interface. The maximum measured operating frequency is 7 GHz at a division ratio of 22, while relevant higher division ratios above 40 increase the operating frequency up to 8 GHz, as shown in figure 7. In this frequency range the divider operates for input power levels of less than -20 dBm. Thus it is well suited for a robust application in the above mentioned phase-locked loops.
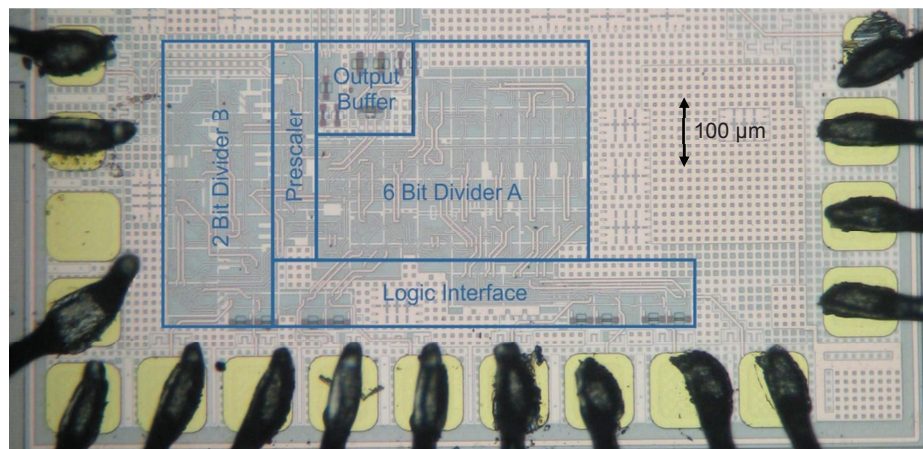

Figure 6: Chip photograph, SiGe bipolar technology (f_T=200 GHz, f_{max}=250 GHz).

V. CONCLUSION

A programmable frequency divider using a dual-modulus prescaler and two synchronous dividers operating with a supply voltage of 3.3 V at a total power consumption of 130 mW have been presented. It is intended for application in millimeter wave FMCW radar systems. The high programming speed allows synthesis of highly linear fractional-N frequency ramps. The divider and the millimeter wave components to be integrated on a single chip will result in a cost, area and power efficient solution for highly precise level radar systems.
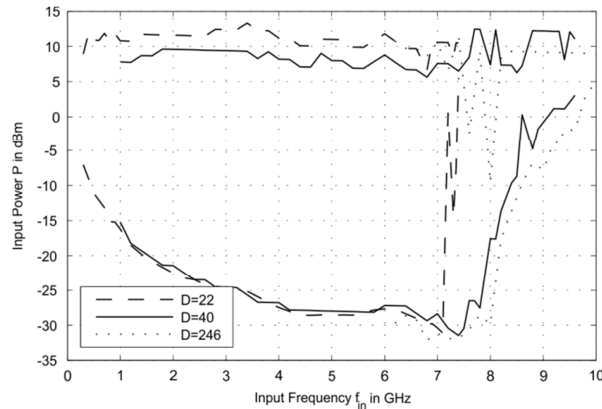
Figure 7: Measured Input Sensitivity for different division ratios N=fin/fout

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