Statistical Analysis of Compensating Properties of Reconfigurable Analog Circuits for Generic Self-X Sensor Interface

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1. Introduction

Nowadays, sensor signal conditioning is very crucial and challenging, as the type and variety of sensors coming into the market are rapidly increasing. Moreover, developing signal conditioning IC's are function of area, cost and robustness to maintain signal integrity. Field programmable analog approaches [1] and the most recent evolvable hardware approaches [2, 3] offers solution for certain extent. Flexibility, and reliability are key issues in designing and operating such systems. However, issues related to fault tolerance and preserving of sensor system performance, quality of registration, and signal processing are not covered by the discussed approaches. The large variety of different sensor principles demands for a large range of sensor electronics interfacing to the sensing elements to perform signal conditioning before conversion to the digital domain. Predominantly, hard-wired solutions with off-the-shelf components are employed, which imply low flexibility with regard to drifts and changes. More recent approaches try to use reconfigurable analog arrays to achieve rapid-prototyping and sufficient flexibility for the sensor electronics. One industrial example is the Vortex family of analog array chips provided by Anadigm Inc., which consist of amplifier and comparator cells and digitally configurable capacitors, that are used as pseudo-resistors and capacitors along with CMOS-switches in the feed-back of the amplifier cells in a Switched-Capacitor (SC) approach. PGA 309 from Texas Instruments is another type of sensor signal conditioning chip available in the market [4]. Moreover, in the field of evolutionary electronics/evolvable hardware, circuits synthesis are carried out by learning procedures on a flexible transistor level granular hardware structure called Field Programmable Transistor Arrays (FPTA). The rate at which novel and new sensor products coming to market and usage are tremendously increasing. Hence development of sensor interface electronics is still a challenging task, which needs special know-how and experience in a multi-disciplinary field of electronics, physics, mechanics etc. However, for the front end communication from sensors to the interface electronics, no standards/general interface electronics for all sensors are available. Therefore optimization of the sensor electronics for the numerous types of electrical signals and sensor characteristics e.g., V, I, C, R, L based-inputs, requires dedicated designs for each of the particular sensor elements. As a result, in spite of the huge industrial interest, the development of sensor systems progresses rather slowly. For example, QuantumX [5] is a discrete product available in the automation market which uses several dedicated types of conditioning for the various sensor type signals, basically working with "one sensor- one Asic" approach. Therefore the main aim of our research work is to address and provide solutions to these problems by combining the sensor industrial demand, and programmable analog arrays with the evolutionary concepts to built a generic, flexible, self-x sensor-interface chips, which are easy to use and can be applied for a wide variety of sensor related products.

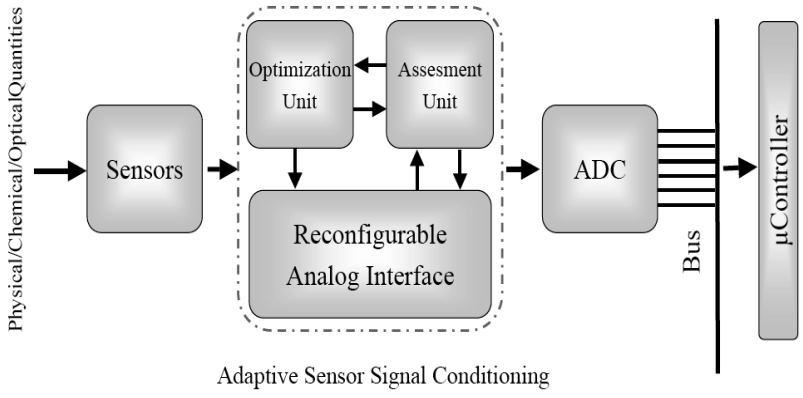


Fig. 1 Functional block diagram of our target generic and intelligent self-x sensor system

The block diagram of the proposed Generic self-x Sensor System is shown in **Fig. 1** [6]. The inclusion of the dynamically reconfigurable generic sensor (multi-sensor) signal conditioner to the smart sensor system illustrates the realization of an adaptive sensor system to overcome some of the hardships of the traditional calibration techniques. The self-x adaptive signal conditioner consists of three separate blocks, namely reconfigurable hardware interface, assessment unit and optimization unit [7].

2. Architecture of the Aspired Generic/Universal Signal Conditioner

Our objective is to implement a standard hardware environment where embedded smart sensors of all types e.g., V, I, C, R, L are pervasive. Although these devices would range greatly in their complexity, the signal processing becomes more trivial. With regard to the aspired industrial application and based on the distilled collection of signal conditioning structures and sizing information from the data sheets (mostly from Analog Devices, National Semiconductors, Texas Instruments, Honeywell and Linear technologies) and along with our design experience, a novel hardware structure had been developed with several Op Amp in different topologies, capacitors, resistors, and switches [7]. The total number of devices, corresponding sizing and/or specification information used to realize various applications circuits were analyzed, classified and remains as a baseline for a meaningful, generic sensor signal conditioning chip. The specifications of the amplifiers used in various signal conditioning circuits are taken from the data sheets of the above mentioned manufacturers.

The architecture of the aspired generic sensor interface electronics is shown in **Fig. 2** (left). The architecture give a relief from optimization of the sensor electronics for the numerous types of sensor signals and its characteristics as they require dedicated designs for each of the particular sensor elements. *"One for all*" concept is here applicable. Based upon our proposed idea of Field Programmable Medium level granular mixed signal Arrays (FPMA) [8] and as an initiative to the above mentioned generic approach, two generations of test chips were designed and tested using 0.35 µm technology from Austriamicrosystems, namely FPMA1 and FPMA2 as shown in **Fig. 2** (right top and bottom). In this paper, statistical analysis and instance specific drift compensation capabilities of FPMA1 are explained. The basic scalable arrays of active and passive elements used to construct established analog circuits like Miller OpAmp, Folded cascode OpAmps and Instrumentation amplifier realized in FPMA1 and FPMA2 are explained in a greater extent in [7]. The three cells on these prototype chips have been provided with three completely separated interfaces, which requires a higher pin count but offers more safety of the work.

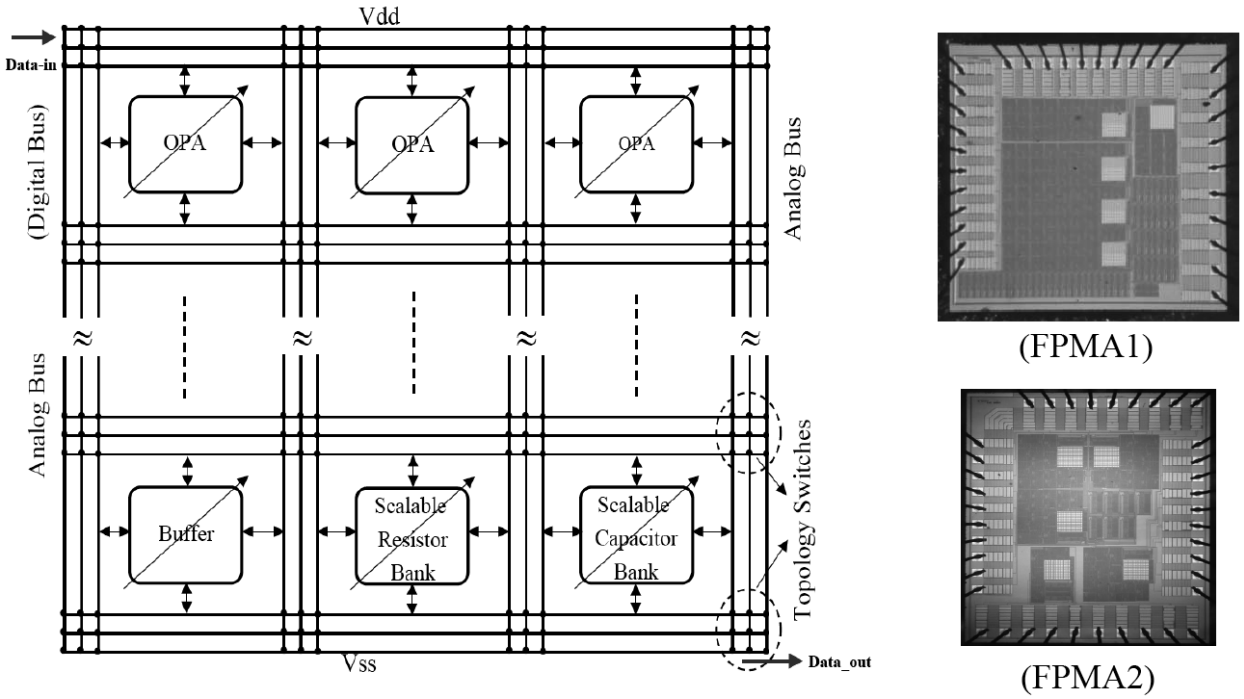
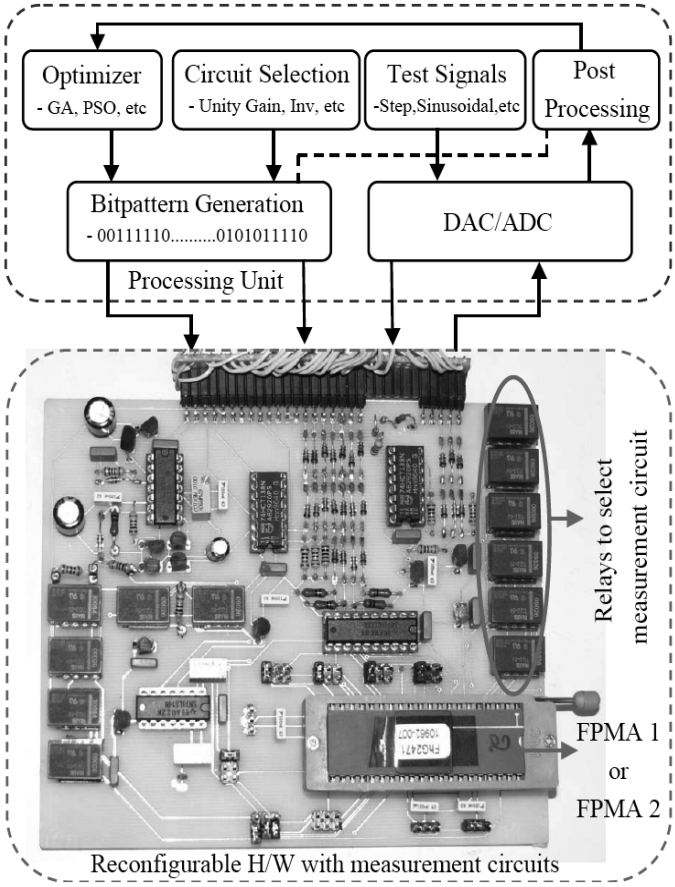


Fig. 2 Architecture of the aspired "One for all" sensor interface (left), post fabricated FPMA1 (right top), post fabricated FPMA2 (right bottom).

3. Measurement Setup

Two different prototypes were used to vadidate the different generation of test chips. The first prototype was a simple 515-C embedded system of PHYTEC, which serves for programming the chip to obtain first measurement results and for advanced analog chip designer training [9]. The system serves to selectively configure the various cells of the chip by clocking in previously prepared configuration patterns, that were generated by manual design activity or extrinsic simulation runs. Various sub boards with different feedback arrangements of the amplifier can be plugged onto the main board with the chip for the common measurement.



Spec_Name	Spec values	Spec weight	Unit
CMR	2.5	10	V
SR_Rising	10e6	100	V/Sec
SR_Falling	10e6	100	V/Sec
Settling time_Rising	1e-6	100	Sec
Settling time_Falling	1e-6	100	Sec
Offset	1e-3	1	V
Output voltage swing	2.5	1	V
Power consumption	1e-3	1	W

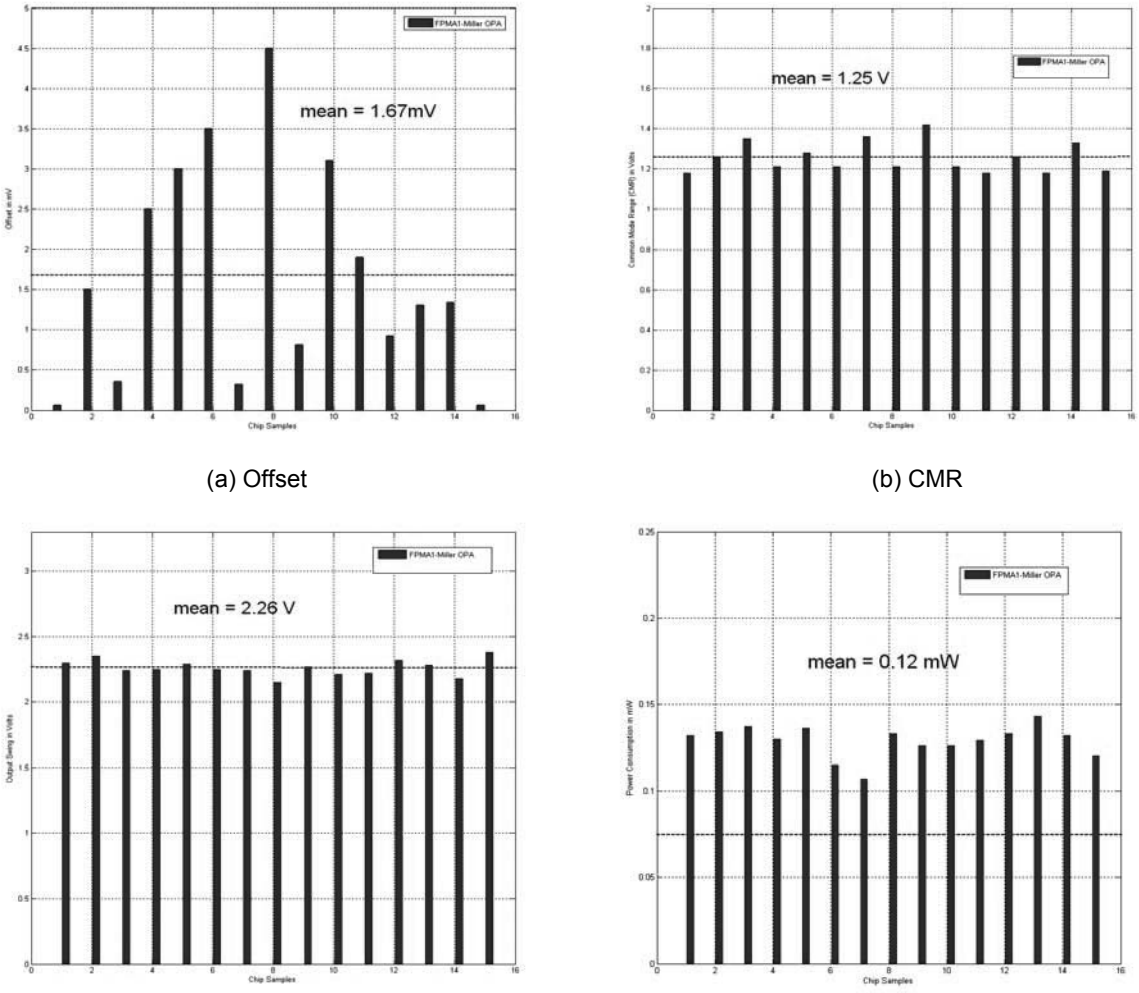
Fig. 3 Block diagram of multi-objective evolvable system developed by Peter Tawdross together with the dynamically reconfigurable hardware platform and assessment circuits (left) and target specification for intrinsic evolution (right).

A second prototype for intrinsic evolution, related to self-reconfiguration or –trimming, has been established in parallel work by Tawdross et al. [10]. The general architecture of the intrinsic evolution environment is shown in **Fig 3(left).** The architecture of this particle swarm (PSO) based multi objective evolvable system mainly consist of two blocks, namely processing unit and reconfigurable hardware along with the measurement circuits. The optimizer in the processing unit runs the bio-inspired algorithms like GA, PSO, etc. Here approaches suitable for dynamic environment were studied and implemented by Tawdross et al [10, 11]. The target specification set at the optimizer is shown in **Fig 3(right).** The device dimensions created by the optimizer based on the fitness functions were then converted to bit patterns and fed in to the designed chips according to the requirements. In this thesis work, we are just the users of his optimisation techniques and works for testing the robustness and statistical analysis of the hardware and thereafter to illustrate the instance specific drift compensation capabilities of the hardware itself.

4. Statistical Performance Analysis and Instance Specific Drift Compensation

Ideally, in a carefully fabricated wafer containing circuits, we would expect all of the circuit on the wafer to be functional. In reality, number of good exemplar might vary from 100% to 0%. The cause of failure can

be due to several factors like, manufacturing procedure, bad design, etc. In case of programmable devices with redundant circuitry, faulty circuits are replaced by switching on to good ones. The statistical properties of programmable devices and the compensation potential so far have not been systematically studied. To the extent of our knowledge, the following brief study tackles this issue the first time. **Fig. 4** and **Fig. 5** show the statistical properties of Miller and FC operational amplifier cells for 15 of 20 samples based on those amplifier specifications amenable to our measurement equipment. Based on intrinsic evolution (see **Fig. 3**) for one dedicated specification a configuration with chip no. 1 was evolved. This configuration was programmed to the other 14 to assess the inherent deviations. With regard to an unbiased procedure, the measurment was repeated five times and mean results are presented. It can be clearly noted from **Fig. 4(a)** and **Fig. 5(a),** that, in particular, the offset variation is significant. In order to compensate the observed variations, all of the 14 test chips in the next step were subject to individual optimization runs from scratch. Five intrinsic runs were carried out for each chip and mean result of five measurements of each of the five obtained configurations are presented. **Fig 6(a)** and **Fig. 6(b)** show the corresponding minimized drift in specification values for the studied hardware cells (Miller OPA and Folded-Cascode OPA). **Table 1** shows the achieved performance improvement.



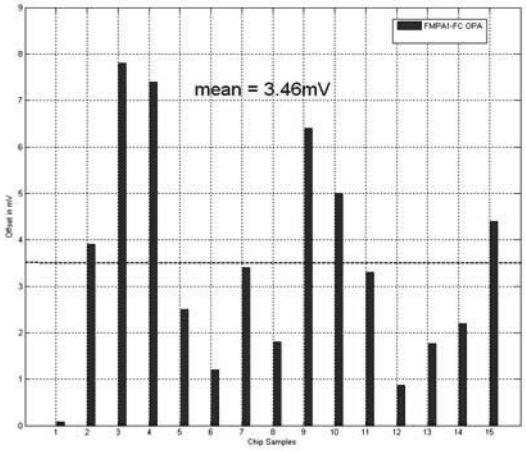
(a) Offset (b) CMR

(c) Output Swing (d) Power Consumption

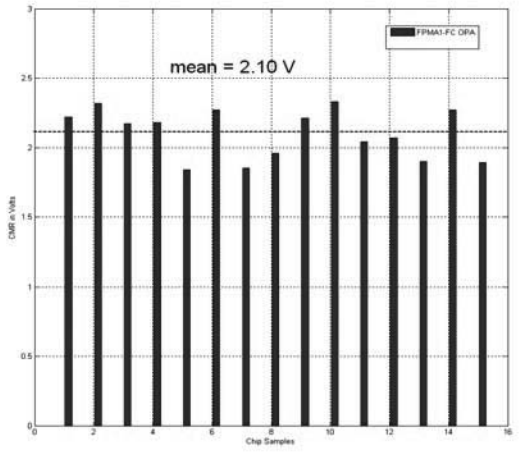
Fig. 4 Statistical comparison of 15 samples of FPMA1 for Miller OPA.

Table. 1 Drift compensation through dynamic reconfiguration

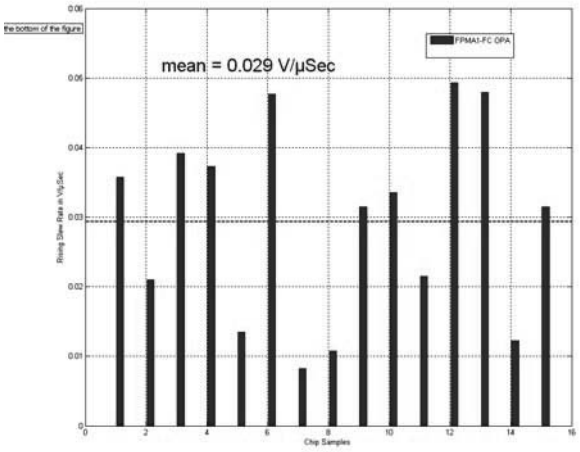
S. Nr	Hardware Implementation	Instance. Spec. Deviations, Σ/N (Offset)	Instance. Spec. Compensation, Σ/N (Offset)	Betterment In % Σ/N (Offset)
1	Miller OPA in FPMA1	1.67 mV	0.48 mV	71.26 %
2	Folded cascode OPA in FPMA1	3.46 mV	0.346 mV	90 %



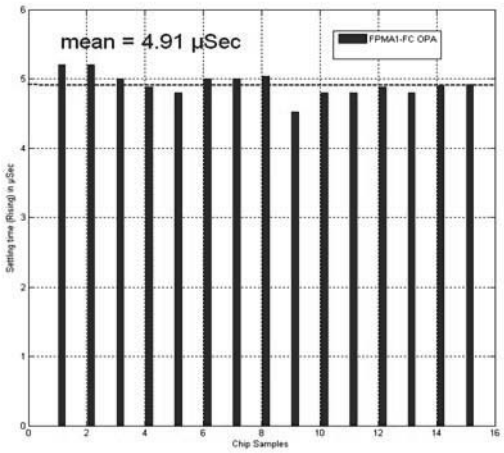
(a) Offset



(b) CMR

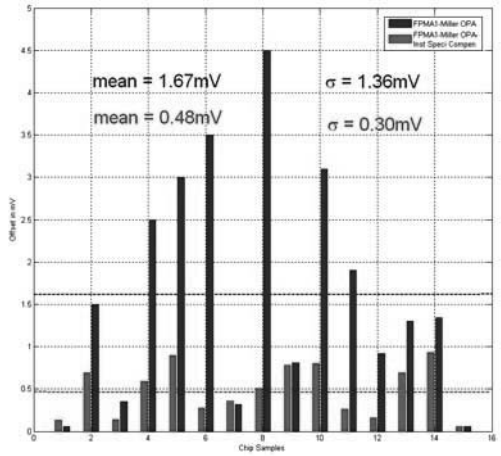


(c) Rising Slew Rate

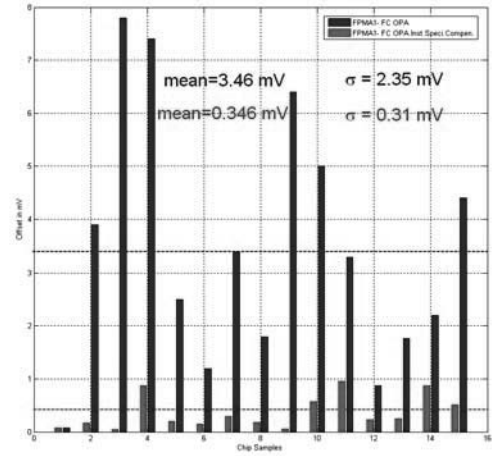


(d) Settling Time

Fig. 5 Statistical comparison of 15 samples of FPMA1 for Folded-Cascode OPA.



(a) Miller OPA



(b) FC OPA

Fig. 6 Statistical comparison showing instance specific deviation in offset and its compensation configurations for 15 test samples of Miller OPA (a) and FC OPA (b) in FPMA1

5. Conclusions

In this paper, architecture of a potential generic, dynamically reconfigurable self-x sensor interface electronics front-end chip was depicted. The proposed architecture is expected to support several sensors of varies types, e.g., V,I,C,R,L based-inputs, and to allow the definition of generic/universal sensor signal conditioning with self-x features like self-trimming, self-repairing and self-calibration. Several established analog circuit structures designed and manufactured in 0.35 µm CMOS technology from austriamicrosystems. The key point in this paper is the application of a prototype system for intrinsic evolution, employing particle swarm optimisation [11], for statistical analysis of the available batch of reconfigurable circuits. Such analysis could so far not be found in the literature, but such analysis results are a crucial prerequisite to assess resource expenditure in reconfigurable chips and industrial applicability of the overall approach. Inherent deviations and compensation potential was studied for selected specification values for Miller and FC OPA of FPMA1. Before compensation, just 40% for miller topology and 13.33% for FC OPA, out of the 15 amplifiers can meet comparable spec values of a standard industrial amplifier (ADA4853-1, AD8018), whereas aftercompensation all the 15 samples can meet the specification. Initially the compared specs are for offset only. This work has also been carried on to the FPMA2, incorporating matching techniques in the layout, which gives better results. Currently, all the statistical analysis bases just on a single specification. In future work, more extensive analysis for various industrial specifications and additional spec values are aspired to obtain a valid assessment of the approach and potential optimisation cues.

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