MHz-Range Interface for Inductive Displacement Sensors[1]

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Abstract- This paper presents a high performance electronic interface for eddy current displacement sensors (ECSs). The interface includes a low-power front-end oscillator specifically designed for high-stability performance. The demodulation principle used to detect the input signal (i.e., displacement information) is explained. A switched-channel technique is utilized to suppress the effect of the offset. Post layout simulations confirm the effectiveness of the design approach as well as the validity of the theoritical analyses. The interface system dissipates 9.5 mW and demonstrates a dynamic range of 16 bits with a 240 µs measurement time and with less than 15 ppm/°C thermal drift over the range of 0-85 °C.

I. Introduction

Displacement/positon measurement is very popular in instrumentation applications because it allows indirect measurement of a number of other non-electrical quantities such as pressure, vibration, acceleration, etc. Among all types of displacement sensors, eddy current sensors (ECS) are often the first choice because of their immunity to variation of environmental conditions like dirt, dust, humidity, pressure, and dielectric properties of the media.

The operating principle of an ECS is based on Lenz's law. Most often ECSs are constructed in such a way that a sensing coil is placed in front of a metallic (i.e., conductive) target. When a metal target is present in a magnetic field and an alternating current is passed through the sensing coil, the electromagnetic induction causes a circular eddy current to flow on the surface of the target on a plane perpendicular to the magnetic field direction. Fig.1a shows an alternating current through a coil inducing eddy current on the surface of a metallic target [1]. On the basis of the equivalent circuit presented in Fig.1b, the simplified electrical model of the sensor is depicted in Fig.1c. Expressions (1) and (2) present the equivalent inductance and resistance as functions of R_c, L_c, R_t, and L_t:

$$R = R_c + \frac{(2\pi f)^2 M^2}{R_t^2 + (2\pi f L_t)^2} R_t \qquad (1)$$

$$L = L_c - \frac{(2\pi f)^2 M^2}{R_t^2 + (2\pi f L_t)^2} L_t \qquad (2)$$

where R_c, L_c, and R_t, L_t, are related to the geometric dimensions of the coil and the target, respectively; f is the frequency of the excitation signal; and M is the mutual inductance between the coil and the target –if the distance x between the target and the coil increases then M drops [2]. In the model, C represents the inter-winding capacitance of the sensor.

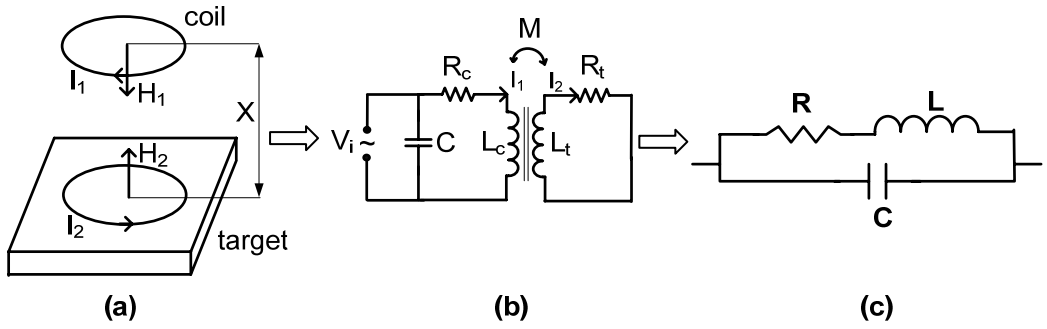

Fig.1. (a) Operating principle of ECS (b) ECS model including an air-core transformer (c) simplified electrical model of ECS.

The electronic interface measures the variation of the inductance, which is related to the displacement. The resistors and the capacitor in Fig.1b are parasitic components, which degrade the performance of the sensor. The parasitic resistance lowers the quality factor of the coil. Also, if the parasitic capacitance of the coil is large then it acts as a short circuit, particularly when utilizing high-frequency signals to excite the coil. As a result, to

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lower the effect of the parasitic components some special considerations should be taken into account when designing the coil as the sensor [3].
There are a number of challenges to be overcome when implementing a low-thermal-drift, low-power, and high-resolution interface for an eddy-current displacement sensor. In some applications there is a need to utilize very thin conductive targets. In these cases the working frequency of the signal exciting the coil(s) should be high enough to reduce the penetration depth of the induced eddy currents to a minimum [1, 3]. Moreover, to achieve a low-power solution, particularly for interface circuits using an oscillator as a front-end stage, the quality factor of the coil(s) *Q* should be high. Therefore, in addition to geometric considerations when designing the coil(s), utilizing a high frequency excitation signal is preferred ($Q \propto \omega$). Other typical requirements for high-performance sensor interfaces are low power consumption, high resolution with a few kHz displacement bandwidth, and high stability. For instance, in a vacuum environment (such as in space) limited means are available to remove the generated heat. Therefore, the interface should be power-efficient and generate as little heat as possible. At the same time it should demonstrate thermal stability if temperature changes. The combined set requirements of high-frequency issues and instrumentation specifications make the design sophisticated.
In recent years some reports have been published presenting high performance interfaces for eddy-current displacement sensors [3-6]. It is worth mentioning that the front-end stage has a very significant effect on the performance of an ECS system.
In [4] a relaxation oscillator is employed to generate a high-frequency excitation signal and also to modulate the excitation frequency with displacement, simultaneously. In the front-end stage an opamp is used which deteriorates the long term stability of the interface. As reported in [4], the thermal drift is in the order of several hundreds of ppm/°C. In [6] a low-power interface system is presented. In this solution a switched-capacitor oscillator, which precedes a band-pass filter, is used to excite the coils. Potentially, the switching operation adds extra *KT/C* noise which is imposed by the series resistances of the switches. In addition, a high-frequency clock is required to generate an approximation of a sine-wave which leads to an increased total harmonic distortion and substrate noise. The high-frequency clock can also contaminate the signal particularly when implementing the system on a chip. As a result, the reported resolution in [6] is not impressive, despite the use of a high-order sigma-delta modulator in the system. In [5] a low-power front-end which includes a few active components is proposed. Such a front-end is potentially capable of developing a high-resolution system because of the limited number of active components (2 transistors). The main drawback of such a solution is its high thermal drift, which is not acceptable in applications requiring high stability. The design approach that is proposed in [3] is mainly applicable in medium-resolution applications.
In this paper we propose an interface system for low-power, high-resolution, and low-thermal-drift eddy-current displacement sensors. Section II presents a low power front-end stage that is utilized to translate displacement to detectable electrical signals. In section III we discuss the circuit design that is utilized to perform demodulation. The switched-channel technique applied to suppress the offset effect is also addressed in this section. Section IV presents the results which have been extracted from post-layout simulations and prototype coil testing. The results confirm the effectiveness of the proposed design approach.

II. Front-end stage

As mentioned above, to convert displacement into a detectable electrical signal, different approaches with various front-end circuits have been reported. The approach proposed in this paper has two main goals: (1) to suppress the sources of drifts without implementing complex front-end circuit solutions and without adding additional performance limitations; and (2) to use signal processing techniques (see section III) which can meet the performance specifications of the system. In [3] an off-chip front-end stage for an ECS system is proposed and conceptually addressed. On the basis of that concept, here we discuss two candidates, which are considered to be partly implemented on a chip, as a front-end stage. Fig.2a shows the first proposal. This front-end stage includes two differential coils as the sensor heads. This improves both the sensitivity to displacement and the linearity. The oscillator modulates a high-frequency voltage with the base-band signal, which contains the displacement information. The output voltages can be simply expressed as $V_{o,+or-}(t) = |V_{o+or-}|.\cos(\omega_c t)$ and

$$|V_{o+or-}| = \eta I_b R_i \qquad (3)$$

where I_b is the bias current, η is the current-switching efficiency, $R_i = Q_i \omega_c L_i$, and *i=1, 2*. R_i is called the single-ended tank resistance [8].
Apparently, R_i is an equivalent resistance which relates to the characteristics of the corresponding coil. The carrier frequency ω_c is approximately defined by the expression $\sqrt{1/(L_1+L_2).C_0 - (r_1+r_2)^2/(L_1+L_2)^2}$ –note that if differential coils are used, then L_1+L_2, and thus ω_c are roughly constant. As mentioned before, L_i depends on the distance between the coil and the target. As a result, R_i, and thus the amplitudes of the oscillator output voltages $|V_{o,+or-}|$, are related to the displacement. Consequently, an amplitude modulation appears in $V_{o,+or-}(t) = |V_{o+or-}|.\cos(\omega_c t)$. Obviously, the noise of the oscillator bias current I_b and particularly its 1/f component can limit the resolution of the measurement system.

In Fig.2a, in order to provide the required biasing current, the current source M_{t1} draws a few mA from the oscillator power supply. Typically, to save power dissipation a large K_m ratio is chosen. Otherwise, the current of M_m would be in the same range as M_{t1}. This causes the current consumption to increase significantly. Unfortunately, large K_m results in amplifying the noise contribution of M_m considerably (see expression (4)). The noise power of the bias current I_b can be written as:

$$\overline{i_{b,n}^2} = \overline{i_{t1,n}^2} + K_m{}^2.(\overline{i_{m,n}^2} + \overline{i_{i,n}^2}) \quad (4)$$

where $\overline{i_{t1,n}^2}$ and $\overline{i_{m,n}^2}$ are the noise power of the corresponding transistors in Fig.2a, and $\overline{i_{i,n}^2}$ is the noise power of the input DC current source. M_{t2} is utilized to improve the total impedance which appears at the source coupling point of the oscillator. It is necessary to mention that the noise of M_{t2} is suppressed by the output resistance of M_{t1} and is therefore negligible.

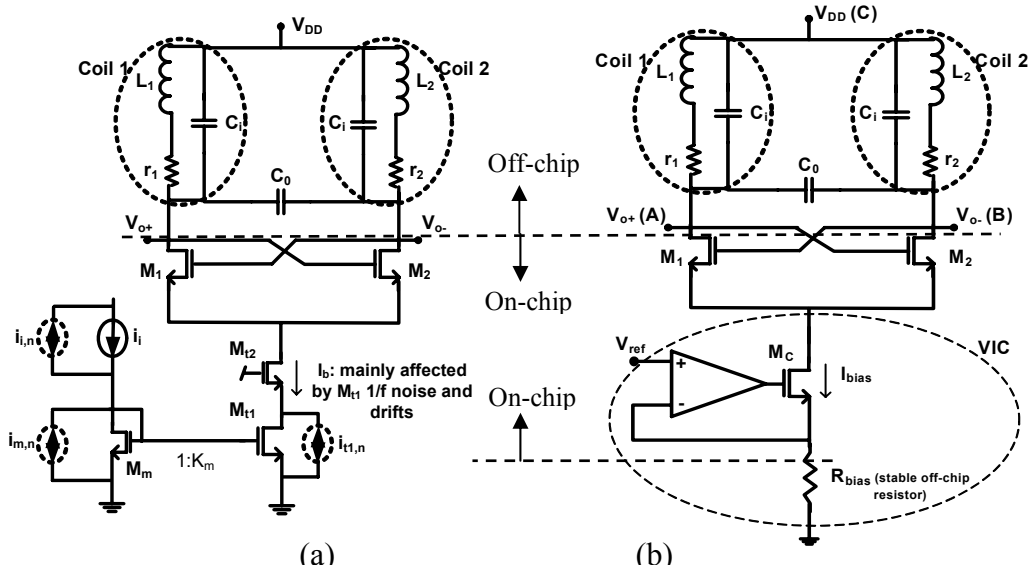

Fig.2. Two candidates for ECS front-end stage; in both cases LC tanks are off-chip
(a) with cascoded transistors (b) with VIC stage as the current source.

To keep the level of the noise power $\overline{i_{b,n}^2}$ low enough (especially the 1/f component of the noise), the straight-forward approach is to significantly enlarge M_m. This results in a large area on the chip being occupied, which thus leads to an increase in cost.

Fig.2b shows the second proposal for the front-end stage. In this design, just as the first proposal, all devices, excluding the passive components, are fabricated on a chip.

As shown in Fig.2b, the front-end oscillator utilizes a voltage-to-current converter (VIC) to provide the biasing current. In this structure the gain of the opamp boosts the output impedance of M_C. The gain/bandwidth of the opamp should be high enough not to degrade the current source impedance at the oscillation frequency. If this happens, the effect of 1/f noise and temperature drift can't be suppressed properly [3]. In this design the total output impedance of VIC is around 40 kΩ at the operating frequency of the oscillator, which is approximately 25 MHz. Simulation results show that this value of the output impedance is high enough to efficiently suppress the effect of drifts, particularly thermal drifts. In the current source a high-thermal-stability reference resistor R_{bias} is used. The reference resistor along with a stable reference voltage V_{ref} guarantee the high-stability of the bias current. The reference resistor R_{bias} also degrades the effect of the flicker noise originating from the opamp. It is necessary to mention that the high-frequency thermal noise of the current source is filtered out considerably by the high-quality-factor band-pass resonator, which includes the sensors. Moreover, in the demodulating stage an integration function additionally suppresses the high-frequency thermal noise.

Based on what we have discussed so far, the second architecture has been selected for two reasons. First, the 1/f noise level introduced by the VIC stage is much lower than that of the cascode current mirror stage even if all other devices in these stages are neglected and only R_{bias} and M_{t1} are taken into account. The level of the flicker noise of the resistors is lower than that of MOS transistors. In particular, thin-film resistors are supposed to be free of 1/f noise [9]. Secondly, the current flowing through the current source is in the range of mA. This causes the overdrive voltage of M_{t1} to rise. Therefore, to ensure that the overdrive voltage of M_{t1} is small enough, its size should be large enough. Based on our simulations, to sink a similar biasing current, the first architecture must occupy a much larger area on the chip. However, the current consumption of the second architecture is slightly higher because of the opamp being used in VIC stage.

III. Demodulation approach

In [3] it is shown that the ratio-metric measurement can improve the stability of the system. The demodulation approach employed in that paper is based on taking two samples simultaneously at voltage peaks to perform ratio-metric measurements. However, such a demodulation technique is mainly applicable for medium-resolution applications. In [3] oversampling and averaging are recommended to improve the resolution. This approach limits the bandwidth of the system. On the other hand, if the sampling capacitance is enlarged to suppress *KT/C* noise, the loading effect of this capacitor on the oscillator may cause the oscillation to stop.
Fig.3 shows our proposal for demodulating the output signals of the oscillator for a 16-bit application. The demodulating part includes three channels. Each channel is constructed by two key blocks, a peak detector [7], and a low-pass filter. The -3 dB frequency bandwidth of the employed opamp is slightly higher than 25 MHz. The peak detector works as follows. If the voltage at the opamp inverting terminal is larger than that of the non-inverting terminal then the output voltage of the opamp goes down. This causes the pMOS transistor $M_{p,pd}$ to be switched on and therefore the capacitor C_{hold} is charged. On the other hand, if the output voltage across C_{hold} becomes higher than the input voltage, the opamp turns off $M_{p,pd}$ because the opamp output voltage rises. Therefore, as long as the input voltage is higher than the output voltage, C_{hold} is charged. This process results in the peak values of the input signal being held. However, because of the gain/bandwidth limitations of the opamp there is an error between the peak value of the input signal and the output voltage. These limitations also introduce voltage ripples at the output. Both the gain error and the non-linear behavior of the sensor can be compensated by calibration and signal processing techniques. The linearity of the peak detectors is about 11 bits, which is higher than the sensor linearity. This linearity was achieved over the range of more than 1 V. A small current source is also introduced to discharge C_{hold} when the value of the input voltage peak lowers. In this design C_{hold} is about 20 pF.

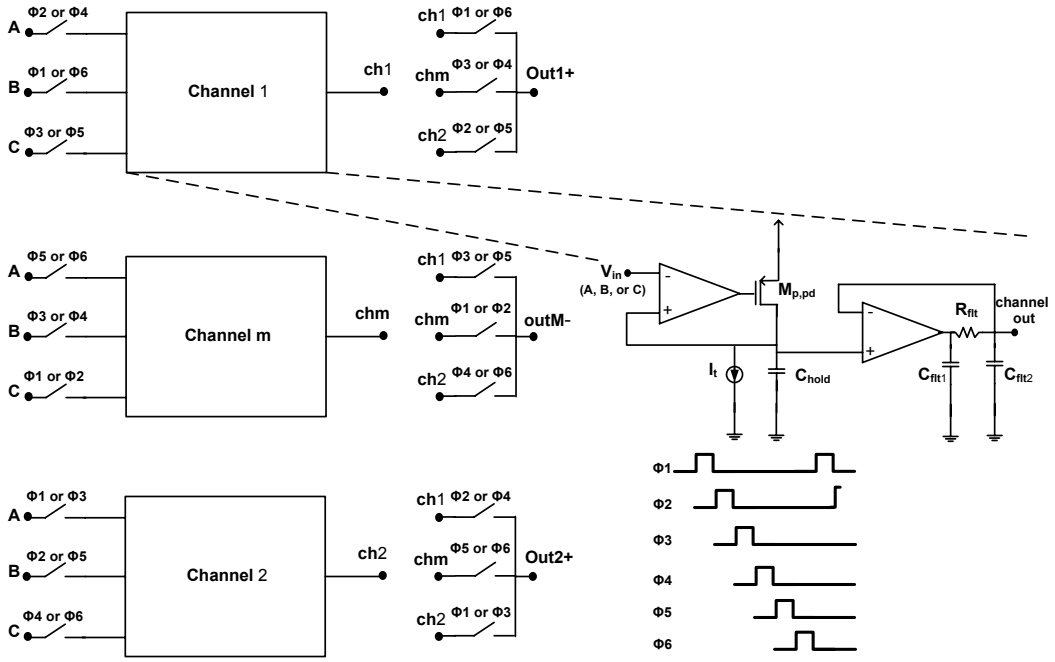

Fig.3. AM demodulator using switched-channel technique to suppress offset.

A low-pass filter follows the peak detector. The low-pass filter is mainly utilized to suppress the very high-frequency ripples about 1000 times. Since the excitation signal frequency is much higher than the signal bandwidth, there is no need for a high-order low-pass filter. The cut-off frequency of the filter is about 80 kHz. This value of the cut-off frequency has been chosen for a few reasons. Firstly, our analysis shows that in order to pass the energy of the input signal (including the displacement information) through a simple low-pass filter with less than a 16-bit loss, the -3 dB frequency of the filter should be at least 40 times larger than the signal bandwidth. Here the single side band of the input signal is assumed to be 1 kHz. Therefore, the cut-off frequency of the filter, which is 80 kHz, is two times larger than the minimum calculated requirement (i.e., 40 kHz). The margin of two is used as a design room. Secondly, to carry out a switched-channel offset cancellation technique each channel should demonstrate several tens of kHz bandwidth. Next, we will discuss the proposed offset cancellation technique. As seen in Fig.3, the demodulator includes three channels, of which one channel is connected to the common terminal of the coils. This channel measures the common mode voltage of the oscillator. Note that the output voltages of the oscillator include the value of the supply voltage as their common mode (CM) level. Therefore, if the supply voltage drifts, it can potentially be

interpreted as a displacement by the system. This happens if the CM voltage is not rejected. By means of a differential structure the common mode voltage variations are suppressed.
As mentioned above, a ratio-metric function is formed in order to attenuate common mode multiplicative drifts to improve the stability of the system. The outputs of the channels are utilized to form the ratio-metric measurement. In order to suppress the effect of channels' offsets, six phases are employed here. At each phase two channels are connected to the oscillator outputs while the other one is detecting the common mode voltage. To do so, during the six phases every channel is connected two times to one of the points denoted as A, B, and C in Fig.2b and Fig.3. The generic function that is made on the basis of the demodulator outputs is:

$$F_{out,dmt} = \frac{(V_{out2+} - V_{outM-}) - (V_{out1+} - V_{outM-})}{(V_{out2+} - V_{outM-}) + (V_{out1+} - V_{outM-})} \quad (5)$$

where V_{out1+} , V_{out2+} , and V_{outM-} are the voltages of the corresponding points shown in Fig.3. In *Φ1* we have:

$$F_{out,dmt,\Phi1} = \frac{(V_A - V_C) - (V_B - V_C)}{(V_A - V_C) + (V_B - V_C)} \quad . \quad (6)$$

If the offset voltages of the channels are taken into account, one can write:

$$F_{out,dmt,\Phi1} = \frac{[(V_A + V_{offset2}) - (V_C + V_{offsetM})] - [(V_B + V_{offset1}) - (V_C + V_{offsetM})]}{[(V_A + V_{offset2}) - (V_C + V_{offsetM})] + [(V_B + V_{offset1}) - (V_C + V_{offsetM})]} \quad . \quad (7)$$

where $V_{offset1}$, $V_{offset2}$, and $V_{offsetM}$ are the total input referred offset voltages of the corresponding channels depicted in Fig.3. Note that the offset voltages are in the range of few mV, which is much lower than the amplitude of the oscillator outputs (e.g., 250-750 mV). Therefore:

$$F_{out,dmt,\Phi1} \cong \frac{V_A - V_B}{V_A + V_B - 2V_C}.(1 - \frac{V_{offset2} - V_{offset1}}{V_A - V_B}).(1 - \frac{V_{offset1} + V_{offset2} - 2V_{offsetM}}{V_A + V_B - 2V_C}) \quad . \quad (8)$$

Likewise, in the other phases we have:

$$F_{out,dmt,\Phi2} \cong \frac{V_A - V_B}{V_A + V_B - 2V_C}.(1 - \frac{V_{offset1} - V_{offset2}}{V_A - V_B}).(1 - \frac{V_{offset1} + V_{offset2} - 2V_{offsetM}}{V_A + V_B - 2V_C}) \quad , \quad (9)$$

$$F_{out,dmt,\Phi3} \cong \frac{V_A - V_B}{V_A + V_B - 2V_C}.(1 - \frac{V_{offset2} - V_{offsetM}}{V_A - V_B}).(1 - \frac{V_{offsetM} + V_{offset2} - 2V_{offset1}}{V_A + V_B - 2V_C}) \quad , \quad (10)$$

$$F_{out,dmt,\Phi4} \cong \frac{V_A - V_B}{V_A + V_B - 2V_C}.(1 - \frac{V_{offset1} - V_{offsetM}}{V_A - V_B}).(1 - \frac{V_{offsetM} + V_{offset1} - 2V_{offset2}}{V_A + V_B - 2V_C}) \quad , \quad (11)$$

$$F_{out,dmt,\Phi5} \cong \frac{V_A - V_B}{V_A + V_B - 2V_C}.(1 - \frac{V_{offsetM} - V_{offset2}}{V_A - V_B}).(1 - \frac{V_{offset2} + V_{offsetM} - 2V_{offset1}}{V_A + V_B - 2V_C}) \quad , \quad (12)$$

and

$$F_{out,dmt,\Phi6} \cong \frac{V_A - V_B}{V_A + V_B - 2V_C}.(1 - \frac{V_{offsetM} - V_{offset1}}{V_A - V_B}).(1 - \frac{V_{offset1} + V_{offsetM} - 2V_{offset2}}{V_A + V_B - 2V_C}) \quad . \quad (13)$$

Mathematically, one can consider the output function of the demodulator as:

$$\overline{F_{out,dem}} = 1/2 \sum_{j=1}^{2} (\frac{1}{6} \sum_{i=1}^{6} F_{out,dmt,\varphi i})_j \quad . \quad (14)$$

Obviously, the sum of expressions (8)-(13) will be free of offset voltages if the rate of offset cancellation operation is high enough. The 1/f noise corner frequency of the demodulator is a few kHz, based on simulation results. The offset cancellation operation is performed at a rate of about 50 kHz which is much higher than the signal bandwidth of 1 kHz. Therefore, the input signal change is negligible only when a few phases of offset cancellation operation (i.e., 6 phases) elapse. $\overline{F_{out,dem}}$, which includes 12 phases of the offset cancellation operation, is made approximately every 240 µs, which is the measurement time of the system. This function is carried out by means of an analog-to-digital converter and a microcontroller that follow the low-pass filters. In addition to suppressing the offset effect, the applied switched-channel approach, which also implies 12 times averaging, can improve the resolution by more than 1.5 bit.
It is worth mentioning that the frequency of offset cancellation is higher than the signal bandwidth and sufficiently smaller than the carrier frequency. As a result, by utilizing the applied technique there is enough time for the oscillator to be stabilized after each switching. Moreover, there is no need to perform additional filtering and no concern about the effect of ripples, unlike the traditional chopping technique. Furthermore, the demodulation part of the system only introduces small parasitic capacitances at the output of the oscillator and thus their effect on the oscillator is negligible –unlike the demodulation scheme presented in [3].

IV. Results

The front-end circuits were simulated by Spectre® utilizing a standard 0.35 µm 3.3 V BiCMOS process. The full-scale displacement range is 1 mm. Post-layout simulations presented a thermal drift of less than 15 ppm/°C, which is a considerable improvement compared to the previous reports. The level of noise is low enough to achieve a 16-bit dynamic range (i.e., about 15 nm). The total power consumption, which includes those of the oscillator, the demodulating channels, clock drivers, and biasing stages, is less than 9.5 mW with a 240 µs measurement time. In Fig.4a the oscillator outputs are shown when the inductance of the coils are 30nH and 10 nH (i.e., the target is at one of the extreme ends). Fig. 4b depicts the outputs of the demodulator for the same case. Simulation results also confirm that the applied switched-channel technique suppresses the offset effect by several hundred times. The layout of the chip, which was utilized to extract the post-layout simulation results, is depicted in Fig.5.

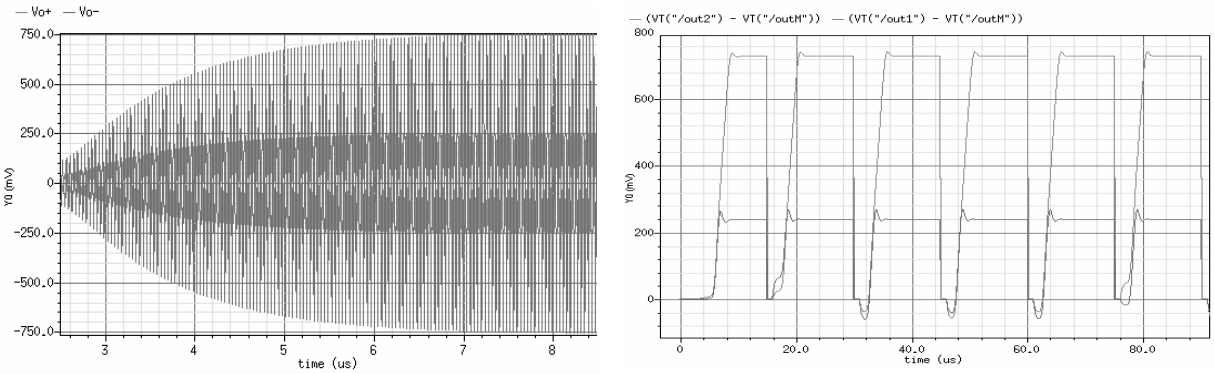

Fig.4. (a) Oscillator outputs for when the target is far from coil1 and close to coil2
(b) differential outputs of the channels performing a demodulation operation.

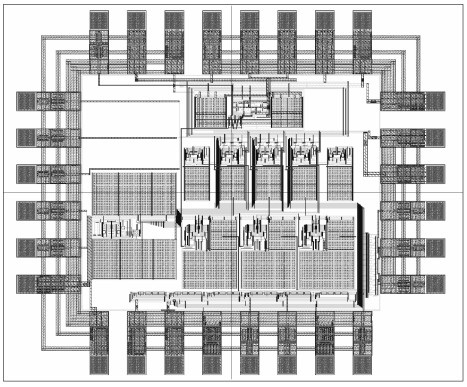

Fig.5. Layout of the chip with an area of 2.3×2 mm^2.

V. Conclusions

In this paper an interface for eddy current displacement sensor has been discussed. The excitation frequency of the sensors is about 25 MHz, which makes it possible to use very thin targets (e.g., with a thickness of a few tens of µm). The resolution of the system is about 16 bits with power consumption of less than only 9.5 mW. An offset cancellation technique, which is suitable for ECS systems utilizing amplitude modulation, was also presented. Next to theoretical analysis, post layout simulations also show a considerable improvement in terms of stability and resolution compared to previous arts.

VI. References

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