Investigation of High-Voltage-CMOS-Technology for the Design of Dynamically Reconfigurable Sensor Electronics

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1. Introduction

The surging advance in microelectronics, predicted and driven by Moore's law, renders ever diminishing transistor sizes, increasing packaging densities and unprecedented complexity of circuits and systems. This is particularly good news for digital designs, however, for analog and mixed-signal sensor electronics, which comprise a small yet essential fraction of a large variety of embedded and integrated systems in industrial application systems, this is less fortunate. In particular, the on-going reduction of supply voltages is detrimental for analog electronics in general. Additionally, interfacing to heterogeneous sensor implementations, the need to deal with higher voltages than 1.8 V-3.3 V might arise. In particular, an rapidly growing variety of sensor solutions becomes available and finds application in a plethora of tasks in measurement, control, automation, and general intelligent systems design. Security or driver assistance systems in the automotive field or monitoring tasks in smart environments and ambient intelligence are lucid examples. In the required embedded or integrated sensor system implementation analog and mixed-signal sensor electronics comprise a small yet essential fraction, which is extremely vulnerable to numerous static and dynamic sources of perturbation (s. **Fig. 1**). Flexibility, robustness, and reliability are key issues in designing and operating such systems.

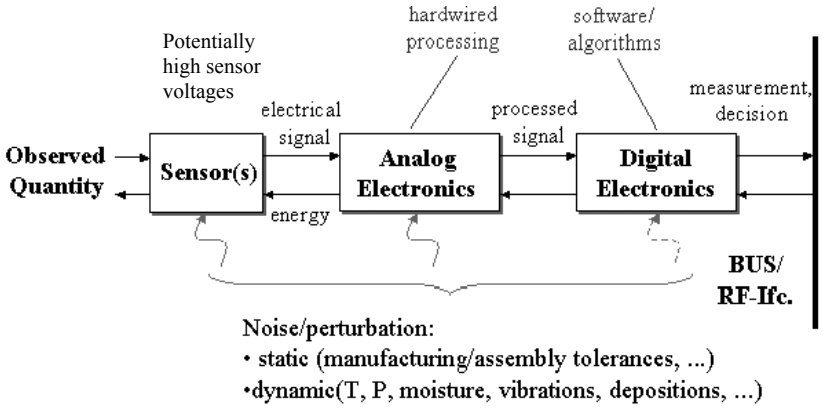

Fig. 1 Principle sensor system with potential source of perturbation and sensor larger than supply voltages

The large variety of different sensor principles and their potential combination in multisensor arrangements demands for a large range of sensor electronics interfacing to the sensing elements and performing early signal conditioning and preprocessing tasks before conversion to the digital domain. Predominantly, hard-wired solutions with off-the-shelf components, implemented in heterogeneous technology and with various supply voltages, are employed, which implies low flexibility with regard to changes and rather slow prototyping. More recent approaches try to use reconfigurable analog arrays to achieve rapid-prototyping and sufficient flexibility for the sensor electronics. Several industrial and research examples can be named, e.g., the Vortex family by Anadigm Inc. [1], the PSOC family of Cypress Inc., the PGA 308 Instrumentation Amplifier from TI Inc., or programmable transistor arrays from the domain of Evolvable Hardware and Evolutionary Electronics [2,3,7]. The existing implementations differ in granularity of the approach, signal representation (time-discrete vs. time-continuous), and resource limitations. They basically all offer the establishing of flexible sensor circuits by programming and even dynamically time-multiplexing between different configurations, which allows to sequentially poll and process different sensors. In prior work, we have studied CMOS implementation of dynamically

reconfigurable sensor electronics meeting industry specifications and having the option of intrinsic evolution for dynamic compensation of deviations and faults [7].
However, all the integrated solutions, including our own previous research [7], are affected by the ongoing supply voltage reduction experienced in main stream microelectronics processes. Similar to PCB level design, it would be advantages to combine higher voltage supply analog units with compact digital processing of contemporary microelectronics. Basically, such heterogeneous technologies are available, as for automotive and other purposes, CMOS processes with high voltage transistors, taking 20-50 Volt, have been developed, retaining the common low-voltage device spectrum.
Thus, in this work the application of such high voltage CMOS technology to create sensor electronic circuits is studied based on a 0.35 μm H35 CMOS process of austriamicrosystems. As little published work in this domain could be found, in the following section the implementation of a basic HCMOS Miller-OpAmp in comparison to the previously designed 3.3 V Miller OpAmp has been examined. This design shows basic feasibility and serves as a reference model for the next steps. In the third section, switch properties, sizing, and implementation in HCMOS will be investigated. Then, the implementation and validation of a reconfigurable Miller OpAmp in HCMOS will be reported. In the last section before conclusions, the status of the physical design, including incorporation of matching properties in the layout, will be given.

2. Sensor Amplifiers in HCMOS

The aim of this work is to assess feasibility and performance of high voltage-based sensor electronics with regard to the competitiveness to the properties of standard industrial electronic cells and components. So far, such investigations and use of high-voltage-technology seems to have been largely neglected. Thus, in the first steps basic amplifier realizations, e.g., Miller-, Folded-Cascode-, or instrumentation amplifiers will be studied and compared in achievable performance, area and power requirements with conventional, low-voltage, i.e., 3.3 V, designs. An additional aspired benefit is an improved signal integrity and noise invulnerability due to the high possible operating voltages. Investigations are based on the H35 (2P/4M) process from austriamicrosystems, where 20 V transistors currently have been preferred to available 50 V transistors from the available spectrum of the technology for reasons of symmetry of applicable voltages as well as reasonable limits of required voltages and power consumption. A Miller OpAmp has been designed in the study using 3.3 V CMOS transistors and 20 V CMOS transistors of the same technology for low and high voltage design, respectively. The design for simplicity based on the heuristic design plan from [6], though evolutionary sizing from previous work [7] can be extended to HCMOS for more sophisticated design, too.

Devices	3.3 V	20 V	S2 20V	S3 20V
M_1	10	20	20	20
M_2	10	20	20	20
M_3	2	2	2	2
M_4	2	2	2	2
M_5	1	1	1	1
M_6	67	59	61	159
M_7	19	19	19	19
C_C	1.63 pF	3.08 pF	6.16 pF	12.32 pF

Table. 2 Sizing results for 3.3V and 20 V Miller OpAmp designs.

Table 1 in the first two columns shows the obtained sizing results, readjusted to optimize simulated amplifier performance, where $M_{1/2}$ are the source-coupled pair, $M_{3/4}$ are the current-mirror load, M_5 is the tail current source, $M_{6/7}$ are the PMOS source stage, and C_C is the compensation capacitor. Appropriate biasing of M_5 is assumed. **Table 2** gives the corresponding simulation results in the first and second column. Obviously, the Miller amplifier design is feasible with slight performance degradation in the first-cut solution and the price tag of considerable increased area consumption and power dissipation.

3. HCMOS Switch Realizations for Reconfiguration

Flexibility, robustness, fault tolerance and reliability are key issues in design and sustained operation of sensor systems. Digital compensation and reconfiguration has found widespread application for this

means. The realization of generic sensor interface IC's [1] and so called self-x sensor systems demands for dynamically configurable analog circuits. This has been regarded in our previous research work [4, 5, 7] and, after basic feasibility check, is currently extended to high-voltage-electronics, to provide rapid-prototyping and self-monitoring and –trimming capability to sensor electronics in high-voltage technology. For this aim, the basic switch behavior of the high voltage transistors had to be examined. In **Fig.2** (left), this is given from the study [8]. The minimum value of 2.05 kΩ is obtained for a minimum width of W=5 μm in a HCMOS transmission gate. It can be reduced for W=10 μm and W=20 μm to 1.1 kΩ and 0.45 kΩ, respectively [8]. For the sake of minimizing node capacitances, the minimum dimensions will be employed in the following [8]. Compared to previous studies, the basic realization of switching resources seems to be even more fortunate in HCMOS-technology**.**

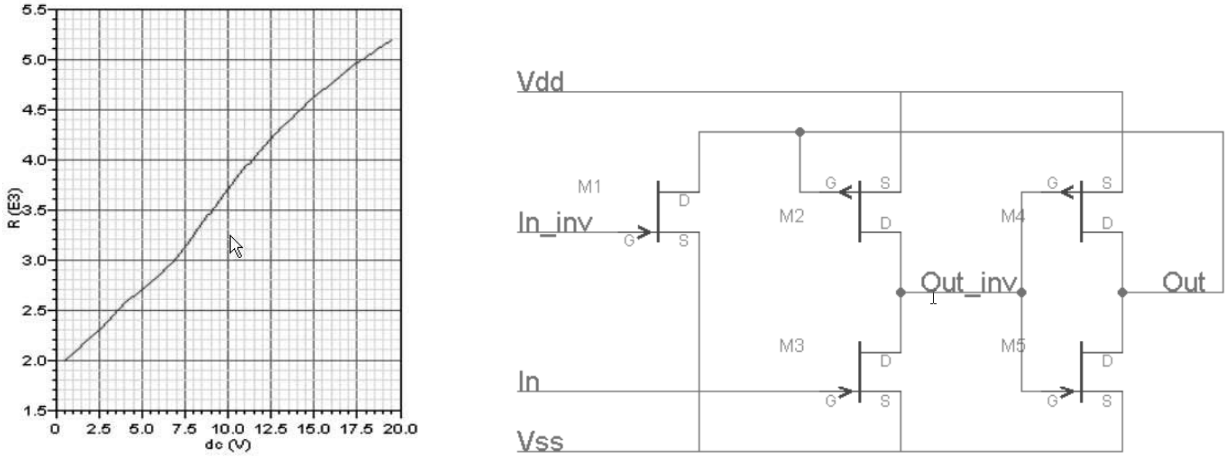

Fig. 2 Switch resistance simulation (left) and switch control circuit (right).

However, the control of these switches from digital configuration memory imposes an additional challenge on the designer. To enjoy compact low-voltage memory, in this case shift register, implementation, the configuration memory bits have to be translated to high voltage switch control signals. **Fig. 2** (right) shows the corresponding translation circuit, which is free of static power dissipation. The design of reconfigurable sensor electronics bases on the design of suitable reconfigurable devices. This elucidated in **Fig.3** (right). Scalable HCMOS transistors, capacitors, and resistors have been designed as in [7].

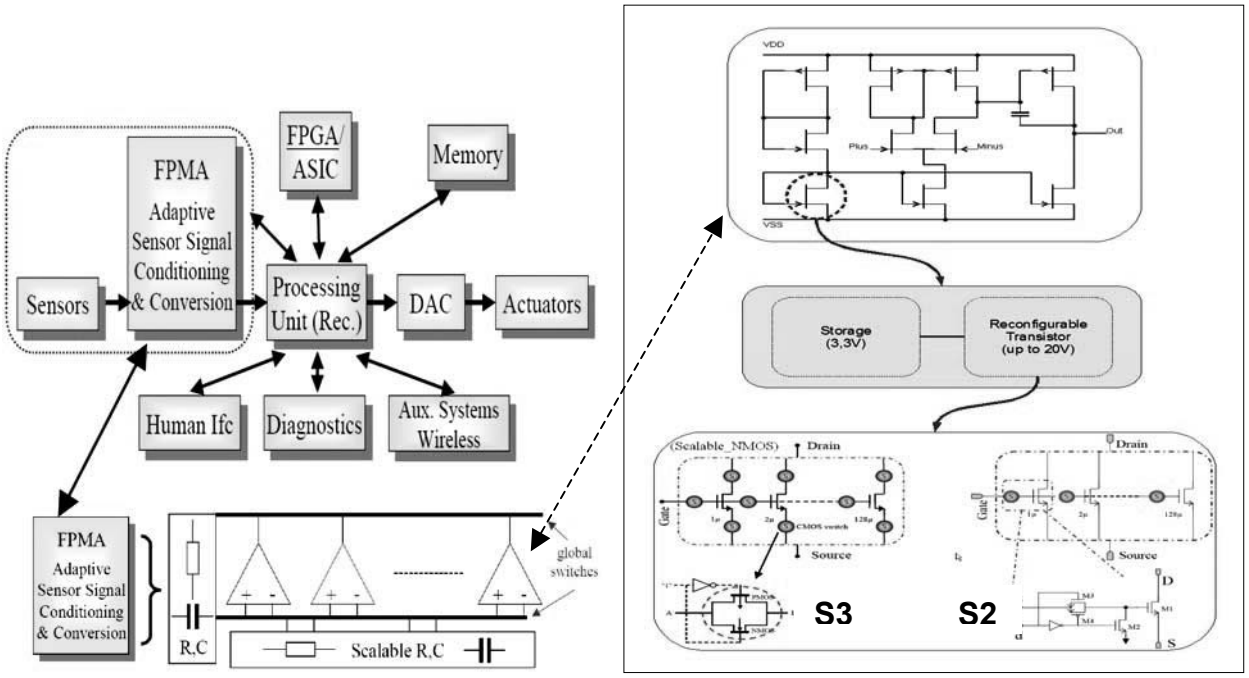

Fig. 3 Concept of generic sensor electronics (left) and hierarchy of reconfigurable devices (right).

With regard to the more fortunate HCMOS switch properties, two common device switch topologies are considered. The **S2** variant for scalable transistors has hard-wired drain and source areas, only gates are switched according to applicable configuration. The **S3** variant completely removes a subtransistor from the array by switching all three nodes. Clearly, the latter variant is more fortunate with regard to fault-tolerance and flexibility, while the first is more fortunate with regard to reducing switch parasitics.

4. HCMOS Reconfigurable Miller OpAmp

Based on the results and sizing hints for HCMOS switches of the previous section and the results of section 2 on the fixed Miller amplifier, two reconfigurable version of a Miller amplifier have been elaborated, based on **S2** and **S3** switch types. Results have again been obtained from schematic simulations (see **Fig. 4**). These have been compared and put into perspective with conventional, low-voltage cell design results with basically encouraging results. Due to feedback from simulations, the HCMOS amplifiers sizing had to be adapted to achieve viable and competitive results. **Table 1** shows in the two rightmost columns the determined sizing for **S2** and **S3** switch types [8]. **Table 2** shows in its two rightmost columns the obtained simulation results of the reconfigurable HCMOS Miller amplifiers.

Specification	3.3 V	20 V	S2 20V	S3 20V
A_{V0}	85.5 dB	70.6 dB	71.6 dB	67.25 dB
GBW	9.35 MHz	5.587 MHz	20.39 MHz	3.43 MHz
A_{C0}	-9.5 dB	-8.5 dB	-8.4 dB	-10.4 dB
CMRR	95.0 dB	79.1 dB	80.0 dB	77.29 dB
φ_R	56.7°	58.6°	59.1°	47.8°
SR	Down: 7.64 V/µs Up: 7.67 V/µs	Down: 23.6 V/µs Up: 24.942 V/µs	Down: 76.6 V/µs Up: 175.83 V/µs	Down: 19.8 V/µs Up: 21.83 V/µs
T_S	68ns	94ns	130ns	196ns
CMR	~100mV – 3.07V	~760mV – 18.1V	~944mV – 18.1V	~880mV – 16.3V
OR	~0 V – 3.24V	200mV – 18.66V	168mV – 18.75V	769mV – 16.61v
U_{OS}	-0,02mV	-0.93mV	-0.52mV	-0.95mV
$P_{diss\ (w/o\ memory)}$	0.933mW	77.64mW	76.08mW	30mW
Area	~500 $(\mu m)^2$	~11000$(\mu m)^2$	~810000 $(\mu m)^2$	~940000 $(\mu m)^2$

Table. 2 Performance results from schematic simulation for 3.3V and 20 V Miller OpAmp designs.

It can be summarized, that the HCMOS technology basically allows to design feasible Miller OpAmps. To further exploit practical suitability for the aspired generic high-voltage sensor electronics, a standard instrumentation amplifier was tentatively investigated on schematic level, based on three reconfigurable Miller amplifiers and the additional seven reconfigurable resistors. The results also show a basic applicability of HCMOS to the design of high-voltage instrumentation amplifiers [8]. The current reconfigurable resistor design, employing a parallel switch/resistive strip topology, however, is very vulnerable to switch on-resistance, in particular for low configured resistance values of the scalable resistor. More sophisticated topologies can amend this problem.

5. Physical Design of HCMOS Reconfigurable Miller OpAmp

Following the schematic level work and result analysis, for the chosen sizing options, physical implementation of scalable devices, including voltage translation circuits, was undertaken for NMOS and PMOS scalable high voltage transistors, scalable capacitor, and scalable resistor implementation. A rather large cell catalogue was designed due to the permutations by the employed switch model (**S2** or **S3**) and matching considerations. In the context of reconfigurable or scalable devices matching becomes an even more complex issue. In the naïve approach, the assumption would be, that mismatch could be compensated by different switch settings if device pairs, e.g., for source coupled pairs, so, obeying matching rules would not be required. However, substrate induced noise or other detrimental effects will affect devices, e.g., transistors in a way, that demands for proximity to achieve compensation. This is supported by previous work and measurement results. Thus, single cells as well as pairwise cells, including matching considerations, were designed and validated. The digital reconfiguration memory has not been physically implemented and added to these layouts, as the investigations target on the analysis of the basic and post-layout behavior of the interesting circuits. The digital configuration memory will have no influence and in the next step of compiling a prototype chip can be more or less copied from the

previous work on 3.3 V reconfigurable sensor electronics circuit. **Fig. 5** shows the first layout of the regarded reconfigurable Miller OpAmp, tailored from the basic scalable device building blocks.

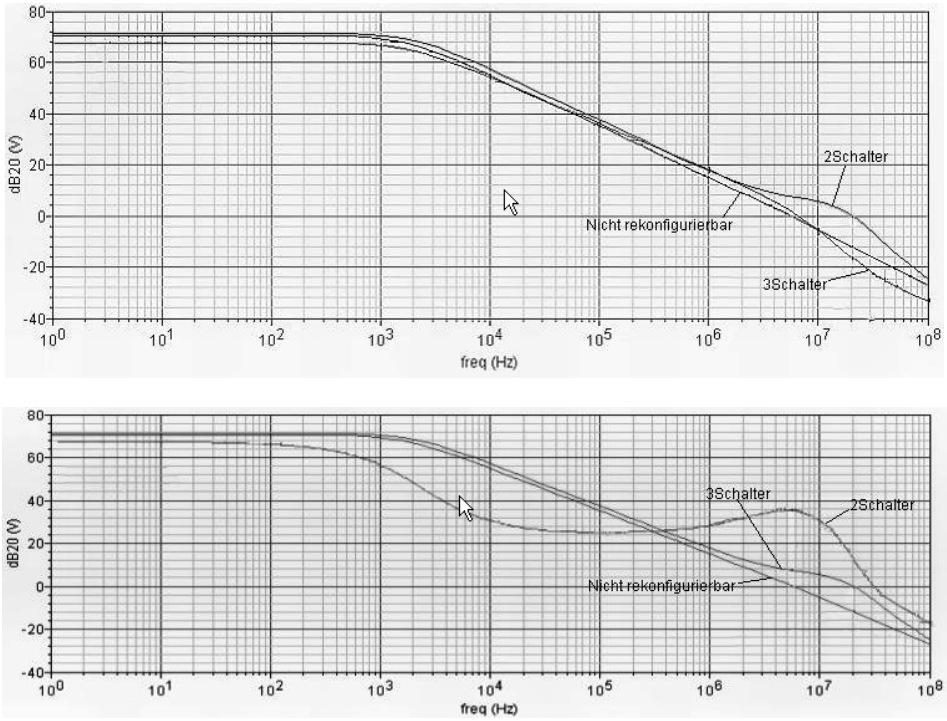

Fig. 4 Bodeplot comparing standard and the two reconfigurable HCMOS Miller OpAmp versions.

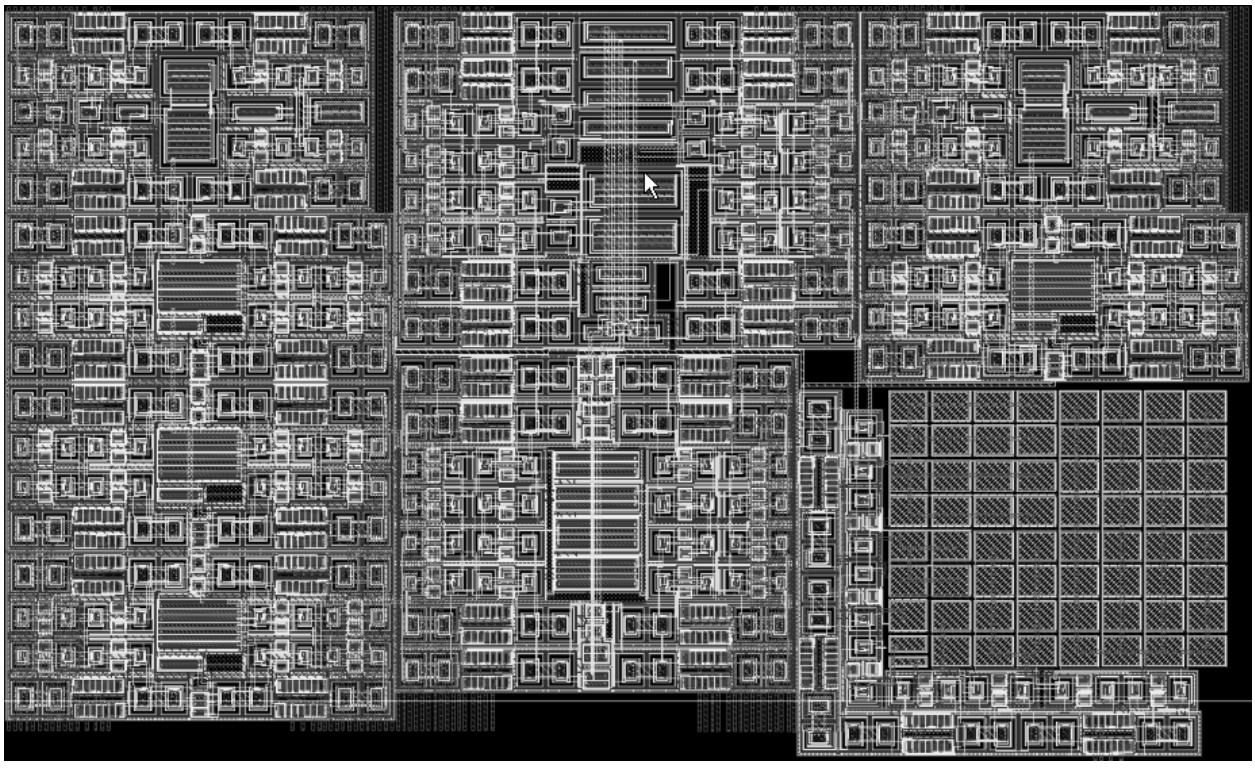

Fig. 5 First layout of reconfigurable HCMOS Miller OpAmp without configuration memory.

The basic scalable cells and the amplifier layout have been subject to design rule check and layout vs. schematic check. Post layout simulation has not been completed due to an unresolved problem in the

employed design flow and tool chain. Resolving this, further cells elaborated in parallel work, e.g., on folded-cascode-amplifier will be integrated with other components, e.g., shift register configuration memory, to a first HCMOS prototype chip with individual amplifier instances as well as instrumentation amplifier and other application circuit instances.

6. Conclusions

In the light of ongoing supply voltage reduction in main stream microelectronics and potential detrimental effects for the design of sensor electronics, the objective of the presented work was to investigate the applicability of high-voltage CMOS technologies for the design of hybrid high/low-voltage, mixed-signal integrated sensor electronic circuits. Further objective was, to investigate the generalization of concepts of dynamic reconfiguration to HCMOS to also obtain generic and potentially self-x sensor electronics and systems.

The first case study [8] gave encouraging results for switch design and showed the basic feasibility of HCMOS Miller and instrumentation amplifier design, however, at the price tag of high area consumption and power dissipation. One more running student project picked up the results and extends the consideration to a HCMOS folded-cascode OpAmp design. The physical design is not completed yet and validation of achieved results based on parasitic simulation and measurement will be pursued next. Due to the compatibility of the 3.3 V and the HCMOS technologies, design experience and even cells from previous designs [7] can be exploited for the aspired HCMOS sensor electronics prototype chip.

Future work, in addition to the completion of physical design and analysis, will have to pick up challenges with regard to design optimization, area and power minimization, and more detailed analysis of the achievable properties, e.g., with regard to signal integrity and noise. A rich variety of hybrid circuit solutions has to be investigated and assessed. To be able to tackle the underlying basic research issues, a DFG grant application will be elaborated.

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