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Cell Optimization for the IISIC CMOS-Chip Serving as a Front-End for Integrated Impedance Spectroscopy

Alexander Renner[1], *Jan Lappas*[1], *Andreas König*[1]

[1] *Institute of Integrated Sensor Systems, TU Kaiserslautern, 67663 Kaiserslautern, Germany,*

koenig@eit.uni-kl.de

Abstract: Distributed data acquisition by integrated, potentially wireless autonomous data loggers ist getting increasingly relevant and applied in many application fields, e.g. in measurement, control, and automation as well as internet of things (IoT), cyber-physical(-production systems (CP(P)S), or Industrie 4.0. Impedance Spectroscopy has established itself as a highly capable, versatile, and increasingly applied method in the sensor, measurement, and instrumentation community as well as for chemical, biomedical, nutritional, and sportive applications. Application requirements on electronics can be met by contemporary desktop equipment but not sufficiently by integrated solutions needed for mobile and hand-held solutions. Thus, in our research, we pursue the design of analog front end (AFE) CMOS-chip that meets requirements as bandwidth of 5 Hz – 3.25 MHz, impedance range of 1Ω – 8 MΩ , etc. identified in our previous application-oriented research, e.g., on hand-held device-based food quality and safety assessment. The cells of the previous Integrated-Impedance Spectroscopy-IC (IISIC) have been revised and manufacturing is aspired to in second half of 2015.

Key words: Impedance spectroscopy, integrated sensory systems, programmable MOSFET-C filters, hand-held autonomous systems, wearable electronics

Introduction

Impedance Spectroscopy has established itself as a highly capable, versatile, and increasingly applied method in the sensor, measurement, and instrumentation community. Applications are ranging from the well-known characterization of electronic devices' properties, the analysis of chemical substances presence and quantity, cell and tissue measurement in biomedical applications or in food analysis and food safety tasks, to the improved reading and diagnose of diverse sensors (e.g., *Lab-on-Spoon* [1], health monitoring in smart watches [6]). The application spectrum imposes very diverse constraints on the measurement set-up with regard to impedance, frequency, DC/AC current, and voltage range, as well as measurement speed, cost, and equipment size. State-of-the-art desktop equipment meets the functional needs, but is too big and costly. Embedded and hand-held solutions on PCB-basis have been conceived with interesting properties and medium size and effort. Commercial chips, e.g., the AD5933 [7], open the door to small hand-held, mobile devices, but is unfortunately quite restricted in its frequency range and other parameters. This work extends and improves the system presented in [4]. Previous work presented in [4] introduced an CMOS-chip, denoted as Integrated- Impedance-Spectroscopy-IC (IISIC), for hand-held application systems with widely tunable AC/DC output currents, for measurements of impedance spectrum from 5 Hz to 3.25 MHz and impedances from 1 Ω to 8 MΩ. Through analysis of the design from [4], weaknesses of several components were identified and optimization, also partially based on automated sizing techniques, and redesign was started. This paper, will describe the improvements, e.g., on the programmable filter units, and give a status of the IISIC design project.

IISIC Architecture and System

The IISIC architecture has seen revision with regard to the overall architecture as well as the individual cells. The programmable filter unit has been completely revised, the voltage-controlled-current-source (VCCS) has been com-

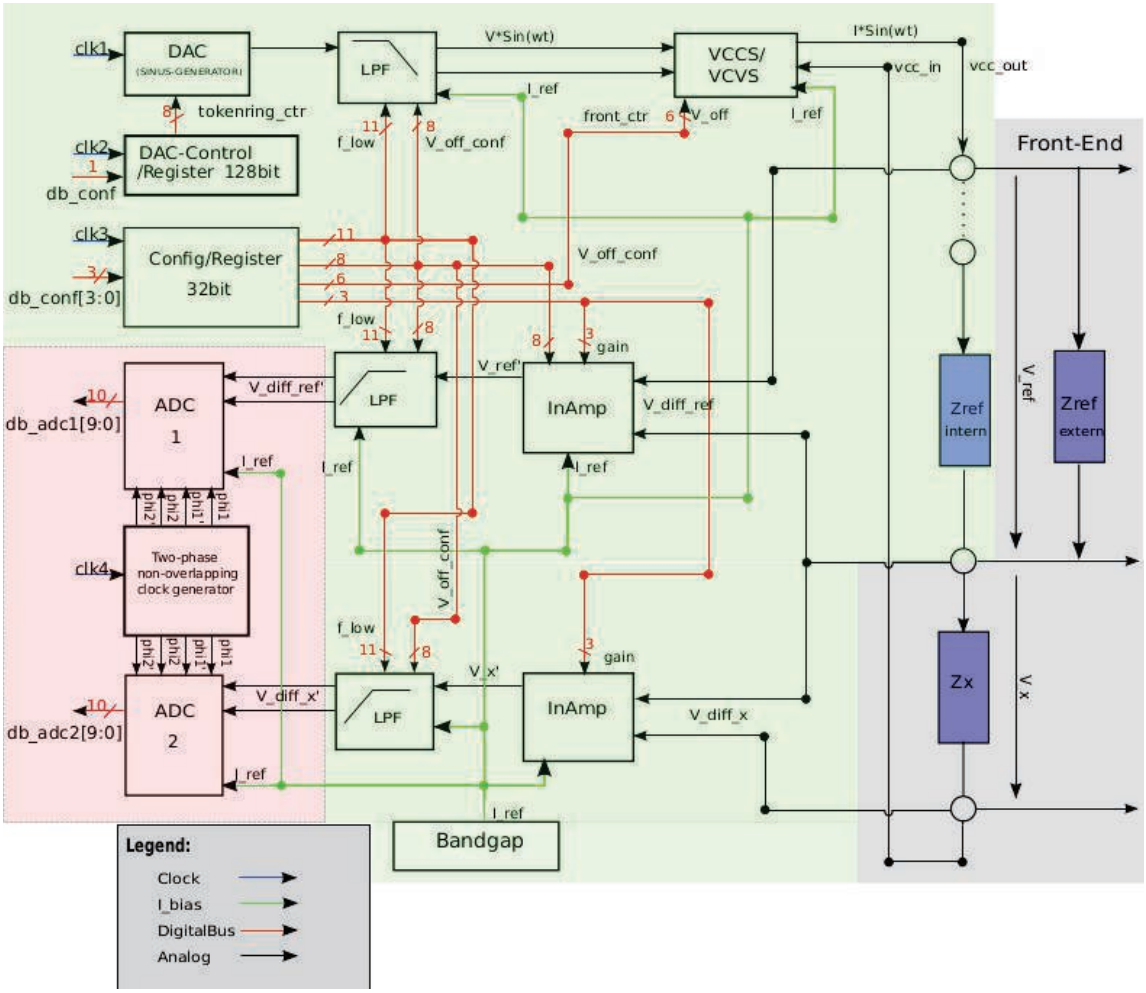

Fig. 1: Revised IISIC block diagram with completed cells given in green, cells in progress given in red, and external components given in grey.

plemented by a digitally selectable voltage-controlled-voltage-source (VCVS). Further, selections for the ADC sampling unit for the 4-wire measurement have been done and the implementation is in progress. Fig 1. shows the block diagram of the revised IISIC including the considerations for the digital control and data acquisition interface. The first version of IISIC will just implement the essentials of the AFE. Testing and data processing of the early prototype will take place on an Arduino based digital front end. This will allow to assess the chips relevant characteristics and is iillustrated in Fig. 2. It can be replaced by a more able digital unit, e.g., FPGA-based, in the next step.

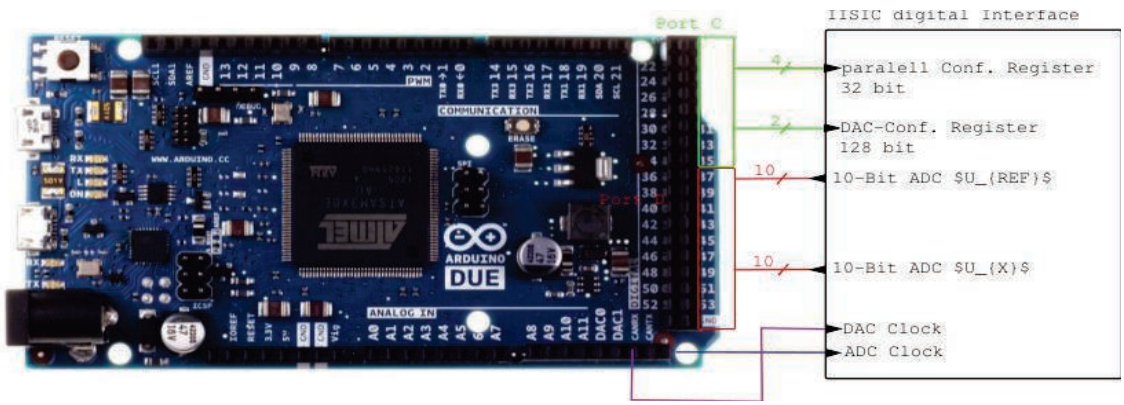

Fig. 2: Block diagram of Arduino based IISIC prototype system with digital interface

Optimized IISIC Cells

MOSFET-C Filter

Due to limitations and problems with the previous gm-based filter, the design of a MOSFET-C-filter was investigated. The new area saving filter is implemented in a differential approach with a 11-bit reconfiguration or 2048 levels for cut-off frequencies from 5 Hz to 5 MHz. Close to 80 dB attenuation are achieved in the chosen filter topology (see Fig. 3, Fig. 4, Fig. 10 (left) and Table 1).

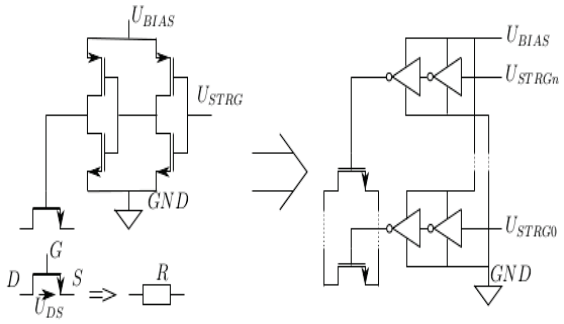

Fig. 3: MOSFET programming cell [4].

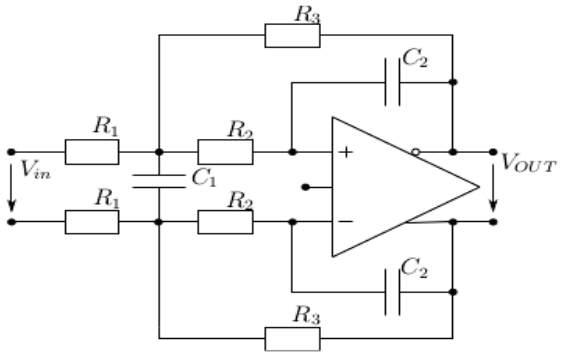

Fig. 4: Differential 2-pole MFB filter [6].

Two circuits of Fig. 4 are cascaded to a 4th-order filter. The cell layout has been completed and is illustrated in Fig.5 This cell will be used three times, as AIF for the sine DAC and as AAF for the two ADC-channels.

Tab. 1: Key performance parameters of the MOSFET-C filter

Min. Bandwidth [Hz]	5
Max. bandwidth [MHz]	5
Gain @ 5 Hz [mdB]	-890
Gain @ 5 MHz [dB]	-2.3
V_{bias} [V]	1.9 – 2.64
P_{diss} [mW]	12.54
P_{PWD} [µW]	800
Reconfiguration depth [bit]	11

Signal Output Stage VCCS/VCVS

In the first IISIC design, exclusively a VCCS has been placed in the output stage, which has an output resistance range from 2 MΩ down to 50 kΩ at 3.25 MHz. The VCCS has been optimized, too, and it has been complemented by digitally selectable a VCVS alternative with an output resistance range from 267 Ω to 332 Ω at 3.25 MHz, which starts to be more effective for larger impedance measurements from 5 kΩ upward, e.g., for oil qualification. Table 2 shows the performance parameters of the VCCS cell (see Fig. 6 and the cell layout in Fig. 7.)

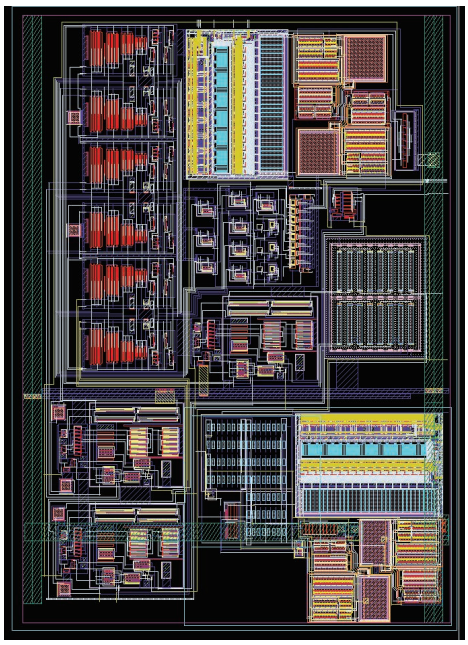

Fig. 5: Layout of 630 µm x 456 µm of the programmable MOSFET-C AIF/AAF filter cell implemented by M. Düntzer

Instrumentation Amplifier

The instrumentation amplifier cell is needed in two copies for the two ADC sampling paths and it has been optimized with regard to possible input voltage range and gain. So it supports a wider range of impedance values in measurement. Fig. 8 shows the layout of the cell and Table 3 gives the instrumentation amplifier's parameters. THD and SNR have been simulated with a low peak amplitude signal of 10 mV at the input and 100 kΩ and 1 pF load.

10-Bit ADC with Pipeline-Architecture

For the ADC conversion a 10-bit converter cell with a maximum clock frequency of 35 MHz and an input range of +/- 1 V with a common mode of 1.65 V from the instrumentation ampli-

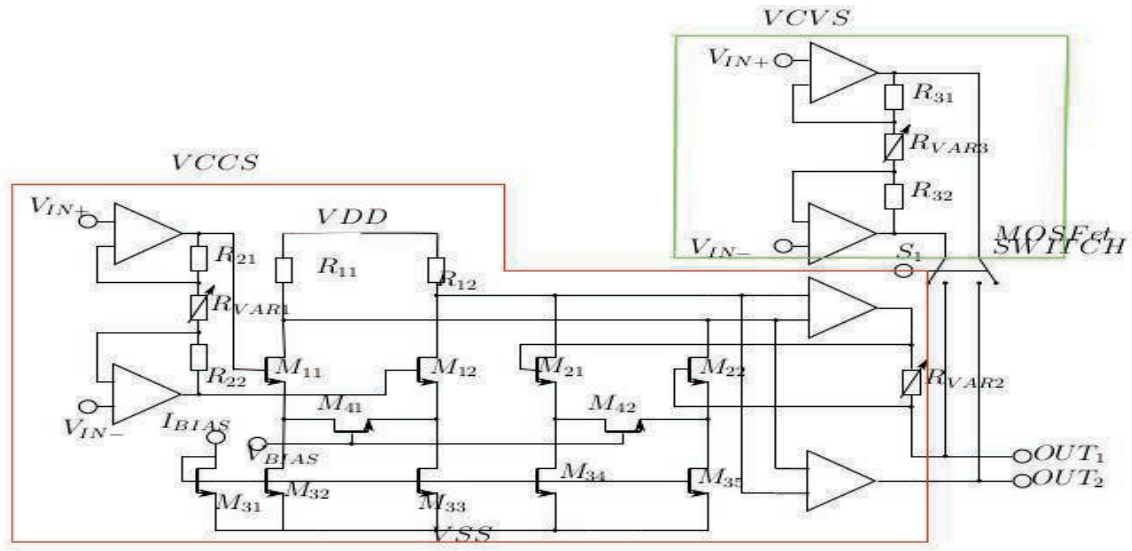

Fig. 6 Simplified block diagram of programmable VCCS/VCVS.

Tab. 2: Key performance parameters of the VCCS

Prog. Stage	1	2	3	4
THD [dB] @ I_{MIN}	-47.58	-45.02	-47.04	-47.67
SNR [dB]	67.9	68.1	68.9	68.48
I_{MAX} p-p [A]	9.6 µ	12.3 µ	119.4 µ	287 µ
I_{MIN} p-p [A]	2.6 µ	4 µ	39.9 µ	96.4 µ
P_{diss} [mW]	79.2	79.2	79.2	79.2
P_{PWD} [µW]	400	400	400	400
Prog. Stage	5	6	7	8
THD [dB] @ I_{MIN}	-47.44	-41.01	-47.65	-44.53
SNR [dB]	67.7	67.6	67.8	67.52
I_{MAX} p-p [A]	1 m	1.36 m	2 m	3.88 m
I_{MIN} p-p [A]	344.3 µ	460 µ	694 µ	1.37 m
P_{diss} [mW]	79.2	79.2	79.2	79.2
P_{PWD} [µW]	400	400	400	400

fiers had to be conceived. A special pipeline architecture [2] was selected and is currently under implementation. Fig. 9 shows a block diagram of the ADC in progress.

Simulation Results

The individual cells have been assessed based on post-layout DC, AC, and transient simulations and the obtained results are given in Table 1 to 3. The whole AFE chain from sine generation to instrumentation amplifier output has been simulated, too, under two restrictions. The required digital signals did not come from the corresponding blocks but from auxiliar sources to facilitate simulations. Further, as the complete layout and the AD-conversion are not yet completed, a schematic-level simulation of the AFE, including the existing cells on post-layout level has been conducted. Fig. 10. (right) shows the results for a DUT.

Conclusions

Motivated by the growing need of sensing, e.g., IoT, CP(P)S, Industrie 4.0, inline measurement etc., a dedicated CMOS AFE is under design [3]. This IISIC will allow a larger group of

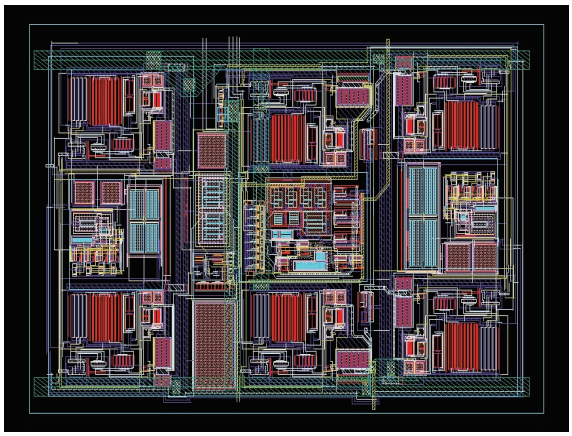

Fig. 7 Layout of 620 µm x 380 µm of the VCCS/VCVS cell.

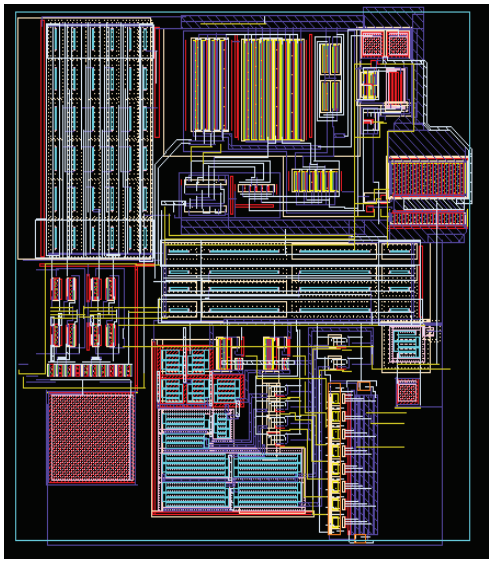

Fig. 8 Layout of 220 µm x 270 µm of the instrumentation amplifier cell.

mobile, hand-held applications with regard to bandwidth and impedance range [1], which are now 5 Hz – 3.25 MHz, 1Ω – 8 MΩ confirmed impedance range, and programmable DC level. The IIISIC is planned to be manufactured in mid 2015 and to be tested and applied in Aduino, based environments, e.g., [1]. Signal processing will be entirely carried out in the digital control unit in this first AFE version of the IISIC concept. After successful validation, integration of the complete functionality will be considered in future work.

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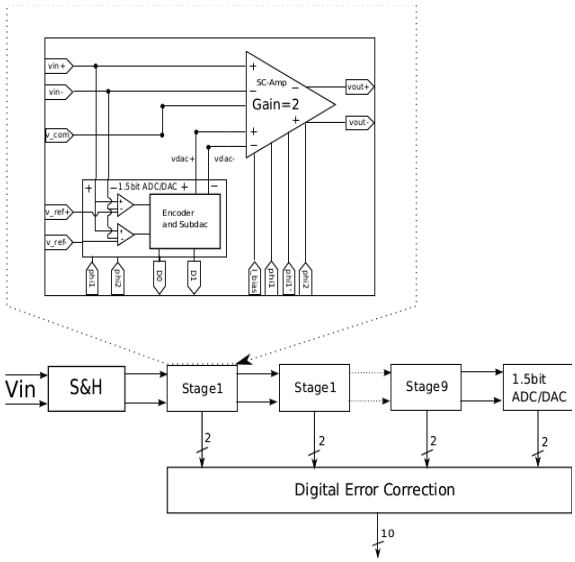

Fig. 9 Block diagram of pipelined ADC.

Tab. 3: Key performance parameters of the instrumentation amplifier cell.

Prog. Stage	1	2	3	4
GAIN [dB]	7	10	12	15
THD [dB]	-51.7	-61.01	-82.46	-84.52
SNR [dB]	72.5	71.39	67.39	66.96
CMRR @ 3.25 MHz [dB]	83.27	82.59	76.79	69.2
CMRR @ 20 Hz [dB]	115.33	112.8	110.7	107.2
P_{diss} [mW]	21.1	21.1	21.1	21.1
P_{PWD} [µW]	300	300	300	300
Prog. Stage	5	6	7	8
GAIN [dB]	18	21	37	43
THD [dB]	-82.75	-72.27	-58.9	-58.9
SNR [dB]	67.7	42.03	37.08	35.9
CMRR @ 3.25 MHz [dB]	65.5	60.75	42.65	37.6
CMRR @ 20 Hz [dB]	105.01	101.6	85.6	80.2
P_{diss} [mW]	21.1	21.1	21.1	21.1
P_{PWD} [µW]	300	300	300	300

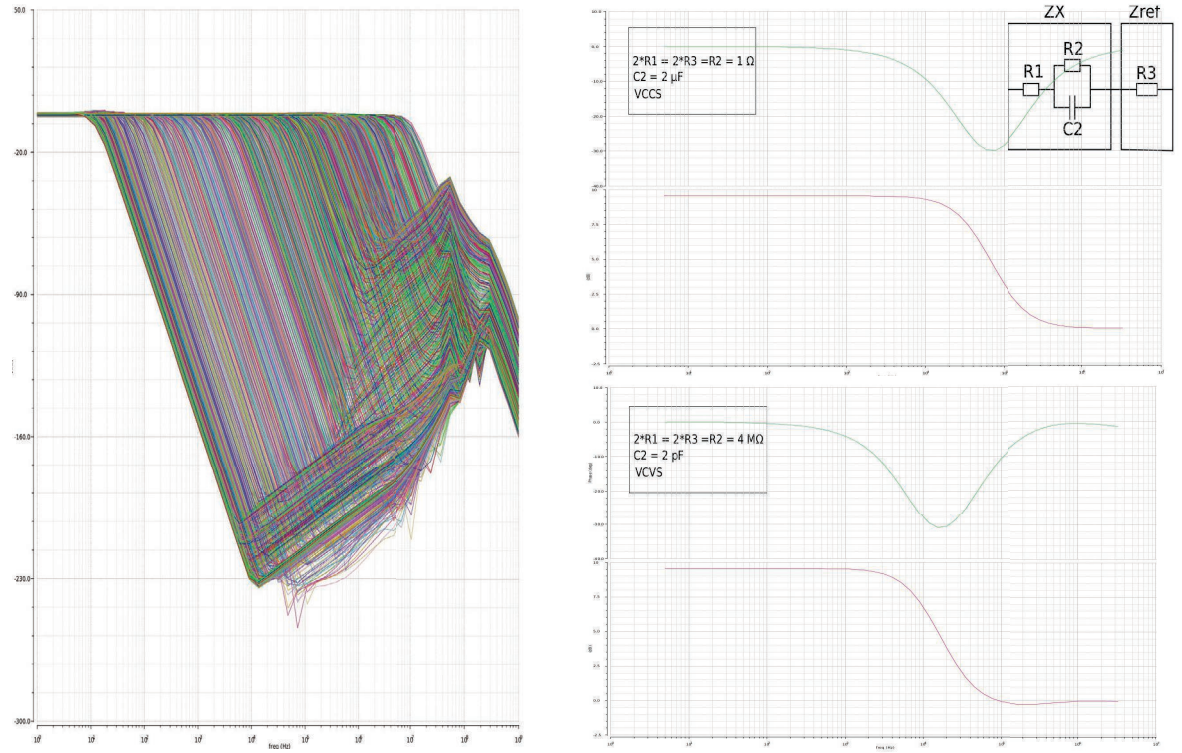

Fig. 10 Programmable MOSFET-C simulation with the corner frequency as a parameter (left) and AFE simulation result from sine DAC to instrumentation amplifiers with a typical DUT (right).