High performance Uncooled amorphous silicon IRFPA with 17µm pixel-pitch

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ABSTRACT
The high level of accumulated expertise by ULIS and CEA/LETI on uncooled microbolometers made from amorphous silicon with 45 µm, 35 µm and 25 µm, enables ULIS to develop VGA and XGA IRFPA formats with 17 µm pixel-pitch to fulfill every applications. These detector keeps all the recent innovations developed on the 25 µm pixel-pitch ROIC (detector configuration by serial link, low power consumption and wide electrical dynamic range). The specific appeal of these units lies in the high spatial resolution it provides while keeping the small thermal time constant. The reduction of the pixel-pitch turns the VGA array into a product well adapted for high resolution and compact systems and the XGA a product well adapted for high resolution imaging systems. High electro-optical performances have been demonstrated with NETD < 50 mK. We insist on NETD and wide thermal dynamic range trade-off, and on the high characteristics uniformity, achieved thanks to the mastering of the amorphous silicon technology as well as the ROIC design. This technology node paves the way to high end products as well as low end compact smaller formats like 320 x 240 and 160 x 120 or smaller.

1. INTRODUCTION

It has been shown that amorphous silicon is definetely well adapted to manufacture in high volume uncooled IRFPAs. From the first product in 2002 with 45 µm pixel size up to 17 µm in 2009, 160 x 120 up to 1024 x 768, easy to use IRFPA are now used in a wide range of applications.
This paper presents our achievement on 640 x 480 / 17 µm and 1024 x 768 / 17 µm sensors. Taking into account previous feedback and analyses, we have paid a special care to design these sensors. The main core technology has not changed but fine tuning on specific parameters has allowed a great leap toward easy-to-handle TEC-less IRFPA.

2. 17 µm UNCOOLED AMORPHOUS SILICON MICROBOLOMETER

2.1 Amorphous silicon

Amorphous Silicon is the base material for uncooled IRFPA. Amorphous silicon presents attractive properties for microbolometer applications. In particular, when it comes to address TEC-less capability, amorphous silicon devices are coping quite well with temperature variation. The bolometer resistance variation versus temperature is described by Arrhenius law in which activation energy E_a depends on the sensitive material.

$$R = R_0.\exp(E_a / kT) \quad [1]$$

As amorphous silicon is not an alloy, every pixels have the same activation energy (E_a standard deviation on E_a mean value < 0.4 %) leading to a high spatial uniformity of pixels temperature behavior. Moreover, amorphous silicon activation energy E_a remains essentially constant throughout a large range of operational temperature. The microbolometer resistance distribution stems essentially from resistance geometry distribution, while remaining stable regarding focal plane temperature variation.
As a consequence, microbolometers' resistances follow a simple and spatially uniform Arrhenius law and hence are fully predictable, leading to easier TEC-less operation with only one gain table for non uniformity correction (NUC) to cover a broad focal plane temperature range.

2.2 Amorphous silicon technology

Amorphous silicon is easy to be monolithically integrated onto silicon substrates at temperature compatible with CMOS integrated circuit. Several key technology improvements are required to successfully scale the pixel from 25 µm down to 17 µm or less. A suitable approach we have follow is first to call for 0.5 µm lithography processing. Advanced lithography in connection with thinner films embodiment clearly give an edge to maintain, and even to improve, the thermal insulation when scaling the pixel to 17 µm while keeping a simple one level microbridge structure which leads to high operability

and high manufacturing yield. This can be achieving without any need for complex and space damaging wrap around and/or meandering leg structures. As a result, legs space arrangement remains quite undemanding and a high fill factor can be maintained. This approach allows to continue to scale a single level microbolometer architecture, taking advantage of a very simple process flow and cost saving.
It is worthwhile to emphasize at this point the technology key benefits afforded by the amorphous silicon option.
Thanks to its silicon like properties, a-Si material has opened the opportunity to design a quite undemanding microbridge structure without any extra feature than the bare minimum required for the bolometer functionality [1]. This leads to a reduced number of technological operations and results in a little number of photolithographic layers. The mere arrangement of the microbridge leads therefore to a fast sensor, featuring pixel time constants largely below the common figures known elsewhere. Although this characteristic mainly depends on the application, it is commonly admitted the pixel response time should not exceed one-third of the reciprocal of the frame time, in other words, 10 ms for an array operating at 30 Hz. The thermal time constant measurements of 17 µm pixels give values under10ms (8.8 ms to 9.3 ms have been measured on the first four 640 x 480 / 17 µm batches) fully compatible with 30 Hz or higher frame rate operation.

3. PACKAGING DESCRIPTION

3.1 VGA Detector

This VGA detector is packaged in a compact (24 x 24 x 4.1 mm^3), low weight (< 6 g) and TEC-less ceramic package. Specific care has been taken to ensure ascendant compatibility with previously developed 384 x 288 / 25 µm sensor. The mechanical and optical interfaces remain the same as ¼ VGA / 25 µm ones and electrical interface is almost compatible with the existing electronics boards (see § 3.2).

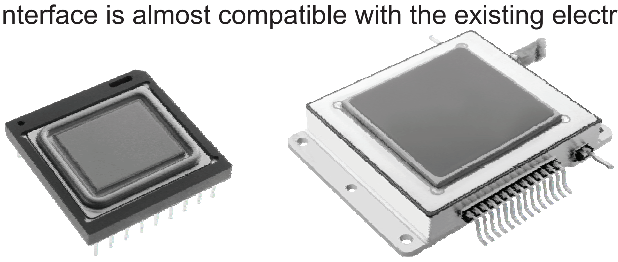

Figure 1: 640 x 480 / 17 µm (left) and 1024 x 768 / 17 µm (right) packages

Regarding the environmental tests, this package design is compliant with the automotive AEC- Q - 100 / Grade 3 standard. Particularly, the detector can withstand high level thermal shocks (-50°C / +125°C - 500 cycles) and High Temperature Storage Life Test (HTSL 125°C – 1000 h).
On the other hand, high combined temperature / humidity tests (95°C – 95 % RH) have been successfully achieved. Several aging and storage tests in progress (> 425 days @ 110°C and 200 days at 170°C, cf. figure 2) are demonstrating a very good package vacuum behavior as computed reliability reaches > 93 % after 15 years.

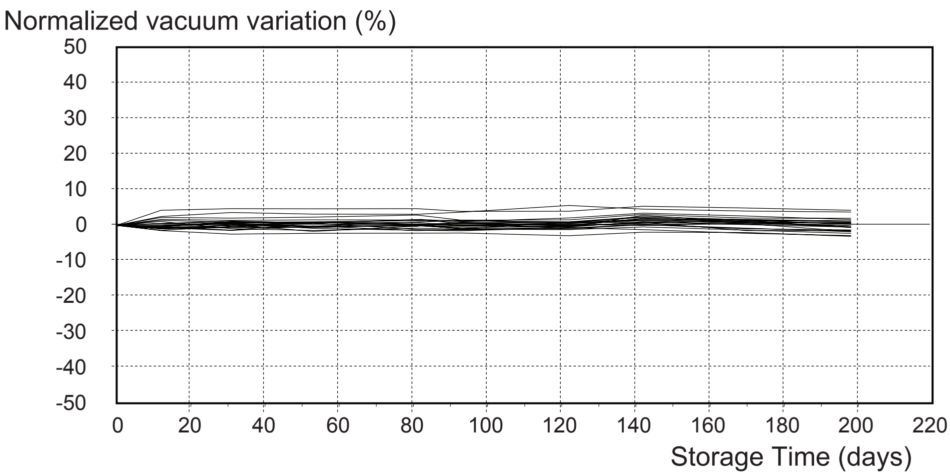

Figure 2: 170°C storage test on ceramics packages

3.2 XGA Detector

XGA package relies on metallic technology in order to offer for this high class detector a possibility to use the package flange as a mechanical reference on which sub part could be integrated (lenses barrel, and/or shutter mechanism). Besides it offers the possibility to proceed to an electrical firing of the internal getter in case of demanding applications.

4 READOUT INTEGRATED CIRCUIT ARCHITECTURE

The readout integrated circuit design includes a serial programmable interface, which allows the operation of the device to be optimized for a wide range of conditions and provides a large degree of flexibility. The array operates in rolling-shutter mode (row by row) with bi-directional scan in both row and column directions. Integration is controlled either by an external clock INT (figure 4) or a programmable instruction in the serial link SERDAT (figure 4). Pixel data of row n are sampled and read out during the n+1 row integration time. Moreover, the ROIC has on chip programmable gain values, which allow optimization of performance over a wide range of operating conditions by tuning integration time and active microbolometer bias. These settings can also be used to optimize or to manage the trade-off between scene dynamic range and sensitivity according to different application.
Moreover, the array size can be controlled with this serial interface. It enables a windowing capability to only select the region of interest and it is possible to refresh this specific area at higher frame rate.

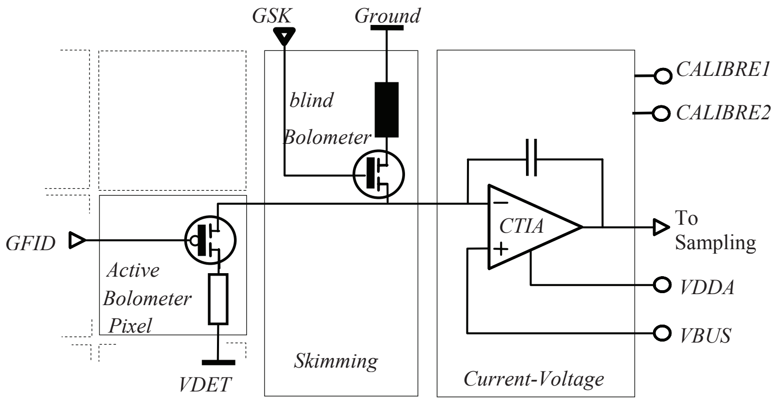

Figure 3: Pixel Readout Architecture

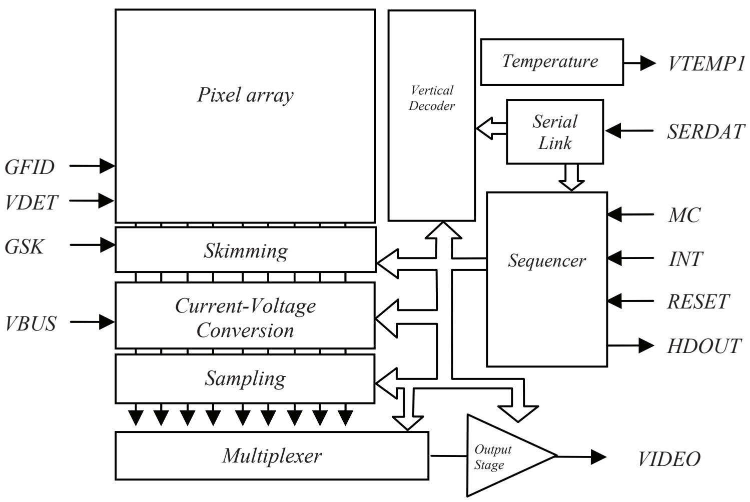

Figure 4: Readout Circuit Block Diagram

4.1 VGA Detector

The ROIC architecture provides a wide electrical dynamic range from 1.4 V to 4.4 V, 30 db power supply rejection ratio and analog output availability. The thermal variations of the infrared sensor due to the scene temperature deviations are presently measured by a current to voltage conversion performed by an integrator (CTIA) in the CMOS readout circuit (figure 3). The trade-off between the sensor performances and the typical scene dynamic range lead us to optimize the combination of integration time and capacitor value in the integrator.

The packaging pin-out is full compatible with the previous TEC-less packaging of the ULIS 384 x 288 / 25 µm pixel pitch product. This readout architecture presents power consumption below 155 mW at 60 Hz operation.

4.2 XGA Detector

The XGA architecture is based on similar concept but two analog outputs have been designed to operate the detector at 50 Hz [3]. However a single output could be used up to 30 Hz frame rate. The ROIC requires 3.6 V voltage biases and therefore the electrical dynamic is ranging from 0.4 V to 2.3 V. Even with two video output amplifiers, this low voltage allows the detector to feature a very low power consumption of only 140 mW for 30 Hz video output.

5. PERFORMANCES AND TEC-LESS CAPABILITY

5.1 Electro-optical performances

Prior to any presentation of the temperature dependence of this new device, we hereafter present the measured performances of one detector. All electrical and electro-optical tests are carried out using f/1 optical aperture and a frame rate of 30 Hz. This device can operate up to 60 Hz. Responsivity is measured using two blackbodies respectively set at 293 K and 308 K. The main characteristics are presented in this section with an ambient temperature of 303 K.

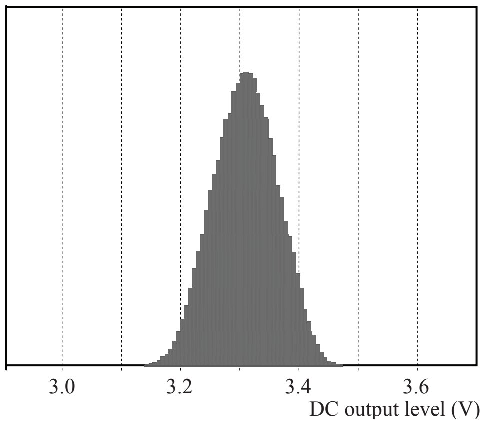

Figure 5: VGA Output DC level histogram @ 293 K

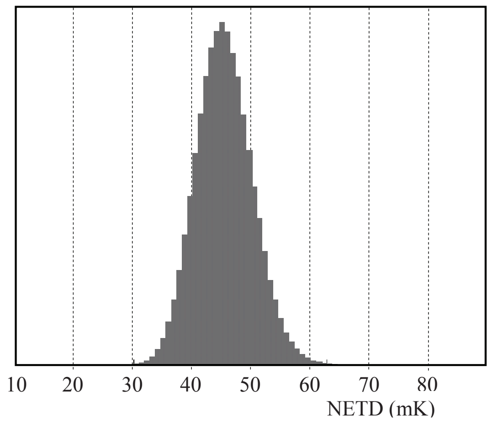

Figure 6: NEDT histogram

The VGA overall output range dynamic is 3 V (between 1.4 V and 4.4 V). The responsivity mean value stands at 12.1 mV/K (operated with 4 pF feedback capacitor of CTIA), hence offering a scene dynamic higher than 150 K for a non linear flux emission of the scene. Figure 5 shows the output DC level for a standard component. The total distribution span (~ 350 mV) represents only 11.5% of output dynamic. The resulting mean NEDT value, @ 303 K of focal plane temperature, stands at 46 mK (figure 6). Residual Fixed Pattern Noise (RFPN) for this component (in TEC-less operation) reaches 295 µV that is 75 % of the RMS noise. The microbolometer thermal constant has been measured between 8.8 ms to 9.3 ms. Keeping this parameter lower than 10 ms is one of our commitment to ensure good image quality at high video frame rate.

5.2 TEC-LESS capabilities

Three main criteria are important to estimate the ability for a circuit to cope with TEC-less operation.

First of all, the DC level is to stay as constant as possible all over the temperature range [3]. Most of all the DC level shall not reach any point of saturation of the circuit. Secondly, the scene dynamic is a rapidly changing variable with ambient temperature; care must be taken not to shorten it at high temperature. Dispersion of the signal and responsivity are the parameters that impact this scene dynamic. Finally, the TEC-less ability is estimated through the variation of NEDT along the ambient temperature range. This figure of merit of an IR detector should also stay as steady as can be with temperature.

DC level stability over ambient temperature change has improved while securing NEDT performance (~ 46 mK). Scene dynamic stays above 100°C for ambient temperature up to 85°C (figure 7).

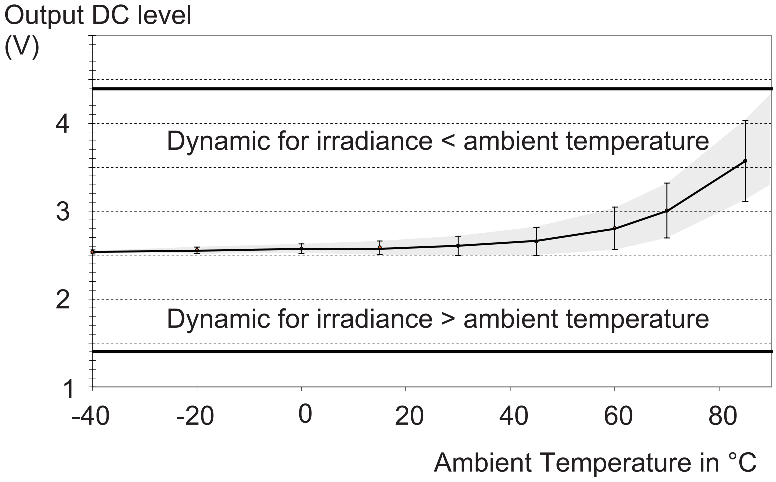

Figure 7: VGA DC level variation with ambient temperature.

5.3 Solar exposure

Solar exposure has been taken into account and these detectors are solar proof regarding usual solar exposure level. Therefore it is not necessary to apply specific maintenance annealing process as it is the case for some other sensitive material [4]. Direct solar exposure on microbolometer leads, whatever the sensitive material is (VOx or amorphous silicon) to a memory effect which disappears with time. The following figure shows the effect of one point correction of the solar induced memory effect on amorphous silicon 384 x 288 / 25 µm microbolometer array. The exposure condition was severe as weather condition was close to Siberian climate: humidity less than 35%, outside temperature is 6°C and the test was performed at 11:00 am with 2 minutes exposure beginning of March (latitude 45th parallel).

9a: Sun trace after 2 minutes exposure 9b: Sun image after one point correction

Figure 9: Effect of one point correction on solar induced memory effect (384 x 288 / 25 µm array)

Even if it is not recommended, this experiment shows that no degradation occurs when amorphous silicon microbolometer arrays are exposed to direct sun. This behavior is similar on the 17 µm devices one.

5.4 IR Images

The optical resolution of the VGA 17µm pitch array matches the quality already available on 1024 x 768 array. The following pictures illustrate the combination of sensitivity and optical resolution that can be achieved.

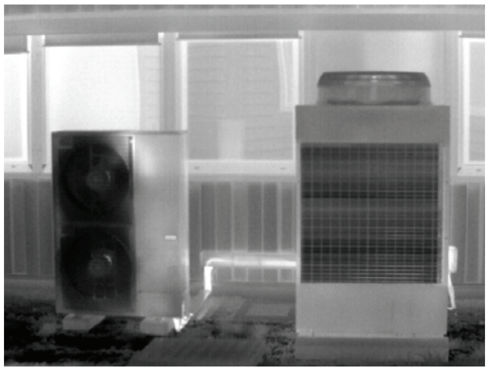

Figure 10: XGA down town image

Figure 11: VGA Heat pump exchanger and fans image

6. CONCLUSION

After having developed the first amorphous silicon XGA arrays with 17 µm pixel-pitch with high uniform performance [4], we have shown that it can be translated in a high performance (45 mK) VGA format sensor well adapted to more compact system with a low thermal time constant (9 ms) enabling 60 Hz frame rate operation with limited smearing effect. The device shows a very low power consumption (150 mW) which allows longer operational time of portable camera or systems. Moreover mechanical, optical and electrical compatibility with QVGA / 25 µm enables easier and faster system upgrade. This VGA / 17 µm sensor paves the way to high volume applications. Taking profit from this small pixel size, future detectors with smaller array sizes ranging from 320 x 240 to lower than 160 x 120, will allow larger number of dies per wafer, leading to decrease the chip cost and to develop more compact systems.

Acknowledgements

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