DOI 10.5162/SMSI2021/D10.3

Adaptive Spiking Sensor Electronics Inspired by Biological Nervous System Based on Memristor Emulator for Industry 4.0 Applications

Hamam Abd[1], Andreas König[1]
[1] Lehrstuhl Integrierte Sensorsysteme (ISE), TU Kaiserslautern Deutschland,
{abd, koenig}@eit.uni-kl.de

Summary:
Modern devices have become more vulnerable to noise as well as to failure with leading-edge technologies. Thus, a spike-processing based ADC design is pursued with promising features, e.g., low-power, low-voltage operation, robust to noise and technology scaling issues. This supports both the self-x properties as well as machine learning in advanced sensor electronics system for practical use in industry 4.0 and IoT. In this work, an adaptive spike-to-rank coding has been designed based on an emulated memristor CMOS circuit, which is the main part of the novel ADC.

Keywords: Spiking neuron, Adaptive spiking sensor electronics, CMOS Memristor, Industry 4.0.

Background, Motivation and Objective

The rapid advance and down-scaling of integration technologies face many issues due to manufacturing deviations, noise, signal swings, etc. This advocates the transition from amplitude coded signals to time-coded signals or spike domain information processing. The memristor spiking neural network (SNN) architecture offers learning, scalability, self-x, noise-robustness, low power, small on-chip footprint, and robustness to technology scaling [1]. SNN has many advantages, however, the memristor is not expected to be feasible in the commercial chip soon, because a lot of open issues , such as compatibility with CMOS technology, unstable switching behavior, the fabrication complexity of memristor systems, and the finite number of resistance levels [1] have to be tackled. To implement memristor SNN on contemporary chips, many researchers have focused on memristor emulators [2]. Inspirations from biological sensory systems can be combined with this approach to advance sensor electronics. Jeffress in [3] had theorized sound localization in human ears. Acoustic localization uses spatially separate sensor pairs to determine the location of the objects. The design of an ADC inspired by such biological sensory systems based on acoustic localization requires two parts. The first one is to generate spikes with the time difference from the sensor is called a sensor-to-spike converter (SSC). The second one will convert this spike to digital and called a spike-to-digital converter (SDC) [4]. Prior work [4] did not make use of adaptivity in the ADC for self-x properties as required, e.g., for Industry 4.0. The primary goal of this research is to design an adaptive spike to rank coding (SRC), which is the main part of the aspired SDC and an adaptive spiking neural ADC.

Proposed Methodology

In this research, the Adaptive Coincidence Detection (ACD) has been designed, which is the main part of the SRC. The proposed ACD design uses two synapses and one neuron, as shown in Fig. 1 A. The synapses have been designed using the memristor from [2], which has been modified to be adaptive, as shown in Fig. 1 B.

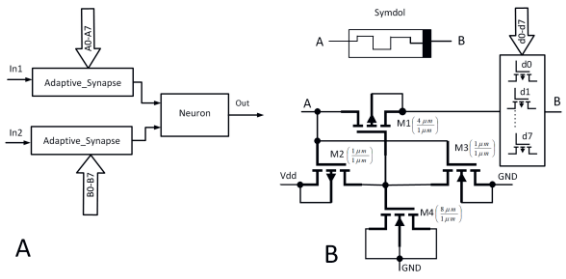

Fig. 1. (A) Adaptive Coincidence Detection. (B) adaptive synapse.

In [5], authors have designed leaky-integrate and-fire (LIF) neuron using memristors. We have designed a neuron using emulated memristor based on a CMOS circuit, as shown in Fig. 2. The memristor circuit in [6] has been modified to serve for the design of a spiking neuron. M1 has been added as a current limiter transistor. C is the membrane capacitor. The

neuron will fire, when the membrane capacitor voltage rises above the crossing point of the inverter. The output is sent back through the delay line (inverter chain) to M6, which discharges the membrane capacitor and limits the width of the spike.

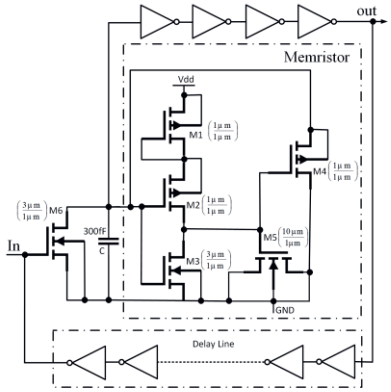

Fig. 2. Implemented memristor-based neuron.

Fig. 3 shows the ACD as the main part of the SRC. SRC shown in Fig. 3 consists of nine ACD. The proposed SDC is designed using Cadence tools and AMS 0.35 μm CMOS technology.

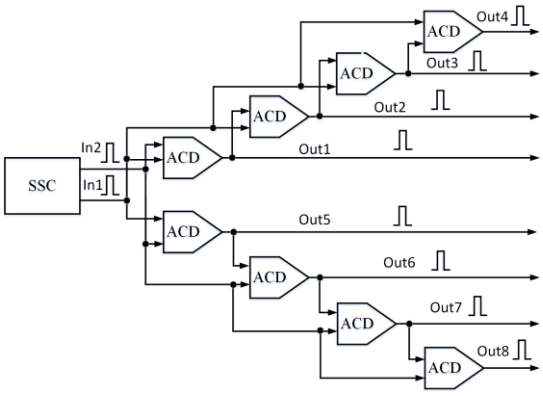

Fig. 3. Adaptive spike-to-rank coding circuit.

Results

Fig. 4 shows for the proposed ACD the three states that usually occur in biological neural networks. The first state generates an output spike if the input spikes arrive at the same time. The second state generates an output spike if the input spikes arrive slightly delayed to each , but the output spike still is generated with delay. In the third state, an output spike will not be generated if two input spikes arrive with significant delay to each other. The currently implemented SRC can achieve up to 5 steps, and each step, the outputs have different order as shown in Fig. 5. The results show that the proposed SRC can generate 2.5-bit value resolution in the digital representation. By increasing the delay chain length and number of ACDs, we can get more bits. However, the upper limit is bounded by the maximum obtainable output order. Fig. 5 shows the rank coding simulation for time differences from 0 ns to 60 ns between the inputs In1 and In2. The SRC performance has been checked under the temperatures (-40 °C, 27°C, 85 °C), and any deviations have been compensated by adapting the synapses weights, which can be achieved by changing the value of the memristor through 8-bit binary digitized transistor. In future work, the resolution will be increased and the design of a complete adaptive spiking sensor conditioning and to-digital conversion electronics be advanced.

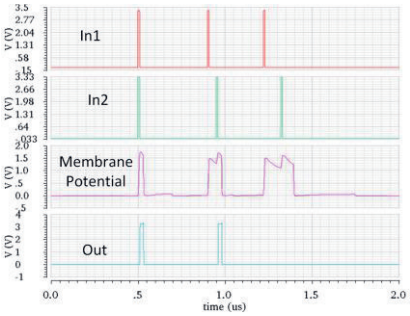

Fig. 4. Adaptive Coincidence Detection simulation.

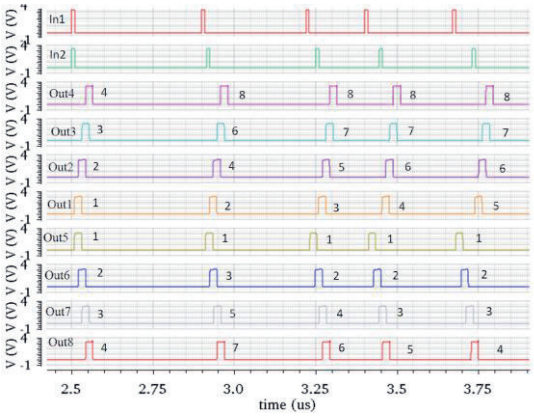

Fig. 5. Rank coding simulation of Fig. 3 SRC circuit.

References

[1] O. Krestinskaya, A.P James, and L. O. Chua. "Neuromemristive circuits for edge computing: A review." *IEEE TNNLS* 31.1 (2019). DOI: 10.1109/TNNLS.2019.2899262.

[2] H. Abd, and A. König. "A Compact Four Transistor CMOS-Design of a Floating Memristor for Adaptive Spiking Neural Networks and Corresponding Self-X Sensor Electronics to Industry 4.0." *tm-Technisches Messen* 87.s1 (2020).

[3] Ashida, Go, and Catherine E. Carr. "Sound localization: Jeffress and beyond." *Current opinion in neurobiology* 21.5 (2011).

[4] Kammara AC, A König. "SSDCα–Inherently robust integrated biomimetic sensor-to-spike-to-digital converter based on peripheral neural ensembles." *tm-Technisches Messen* 83.9 (2016).

[5] Z. Wang, et al. "Fully memristive neural networks for pattern classification with unsupervised learning." *Nature Electronics* 1.2 (2018).

[6] Y. Babacan, A. Yesil, and F. Gul. "The fabrication and MOSFET-only circuit implementation of semiconductor memristor." *IEEE TED* 65.4 (2018).