Low Power Design for Wireless Instrumentation

Yannick Maret, Daniel Schrag[1], Richard Bloch
ABB Switzerland Ltd, Corporate Research, Segelhof 1K, 5405 Baden Dättwil, Switzerland

[1] Formerly with ABB, now with Mettler Toledo, Heuwinkelstrasse 3, CH-8606 Nänikon

Abstract

An intrinsically safe and self-supplied wireless adapter has been developed for HART devices. The adapter works with a supply voltage down to 1.4V and a supply current as low as 3mA. To achieve this, analogue and digital low power design approaches, a new intrinsic safety concept, and a novel control scheme are used. The proposed adapter is connected serially to the 4...20mA loop and harvests energy thereof to supply itself. The voltage drop generated by the adapter should be minimised because the wiring is often close to the maximal allowed length. The voltage available to the field device is minimal at 20mA and maximal at 4mA. All in all, the maximum power that can be used by the adapter is just a few milliwatts. On the one hand, this paper presents techniques to optimise the power consumption such as: efficient and adaptive low voltage and low power conversion scheme based on off-the-shelf components; leakage-optimised large capacitive banks (in our case, 6mF). On the other hand, we also present our innovative solution for low voltage intrinsic safety barriers. At -40°C, the latter achieves a voltage loss of about 200mV compared to the 800mV required for the conventional diode-based solution.

1. Introduction

In the field of industrial automation, the analogue signaling technology known as 4…20mA-loop is widely used. The basic current loop setup is composed of a voltage supply and a signaling device. The latter transmits measurement or control values by modulating the current between 4 and 20mA; any device connected in series to the loop can read the current and, incidently, the transmitted value. Most 4…20mA current loop field devices include Highway Addressable Remote Transducer (HART) communication capabilities [1]. The HART communication protocol is designed to complement the analogue signaling by adding digital signaling capabilities based on a Frequency Shift Keying (FSK) scheme. Unfortunately, HART communication is often only used during commissioning and most setups provide no HART infrastructure. Consequently, much valuable information, such as process or diagnostic data, is unavailable. A wireless adapter is a small device that easily enables this stranded communication on already existing field devices installations [2]: it acts as a bi-directional bridge between wired HART data and wirelessHART. To minimise installation and maintenance costs, the wireless adapter should be self-powered. If serially connected to a in-place 4…20mA loop, the wireless adapter is able to extract enough power to supply itself by creating a voltage drop on the current loop. This voltage drop actually acts as an additional voltage loss for the loop and should be small enough not to disturb existing devices. The principle is exemplified in Figure 1. The available power is thus rather constrained and management thereof is a key element for a successful wireless adapter.

This paper presents different approaches that aim at reducing the power consumption of the developed adapter, or at limiting its impact on the existing 4…20mA loop. The latter is mainly achieved through a novel adaptive voltage drop regulation and by using a new blocking barrier circuit. The power consumption decrease is achieved by reducing the current leakage of the capacitors bank and by optimising the relevant parts of the design.
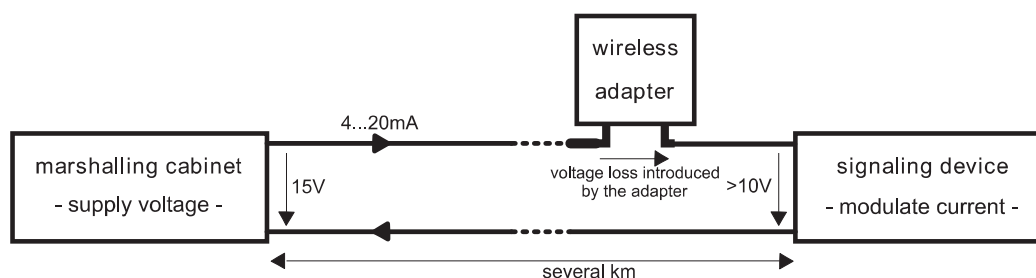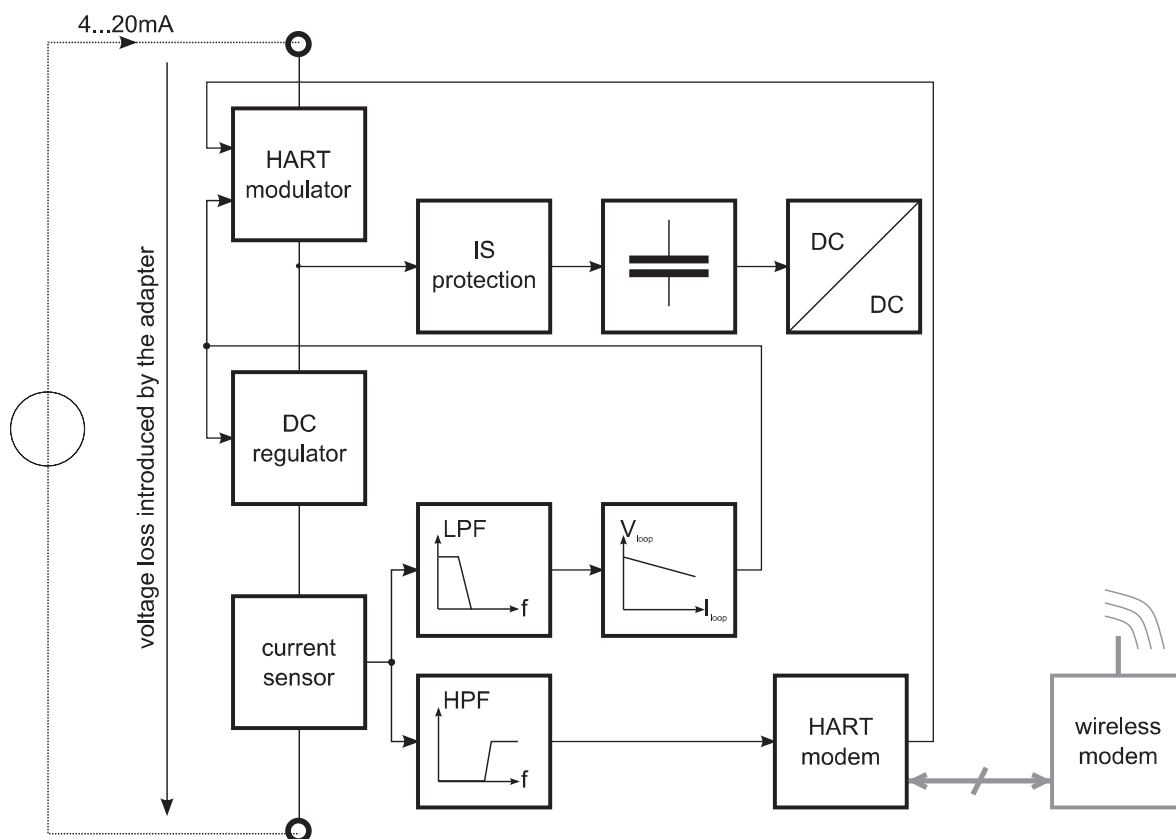

Figure 1, retrofitting of a wireless adapter

Figure 2, block diagram of the wired front-end

The rest of the document is organised as follows. In Section 2, we first give challenges related to the development of a wireless adapter. The remaining sections are structured around the wired front-end of the said adapter, whose overview is depicted in Figure 2[1].The wired front-end primarily consists of a HART modulator and of a DC voltage regulator. The HART modulator takes care of the HART protocol modulation and also regulates the DC voltage drop created by the adapter. On the other hand, the DC regulator creates a stable DC voltage that can be fed to the DC/DC step-up converter. More details about the voltage drop regulation, and its adaptation to the signalling current, can be found in Section 3. As well shown in the block diagram is the power part and consisting of an intrinsic safety blocking barrier, described in Section 4, and a 6mF capacitors bank, described in Section 5. The resulting power consumption and possible improvements are discussed in Section 6.

2.   Challenges

The power available to the adapter is given by the minimum loop current multiplied by the voltage loss created on the loop by the adapter. Since the voltage drop should be minimised, the power is rather constrained: e.g. 6mW for a voltage loss of 1.5V. A wireless adapter is an energy harvesting device: it is powered by a process not designed for that purpose, i.e. the in-place 4…20mA loop, and the peak power is limited.

A device complying with intrinsic safety has the significant advantage that it can be operated in the presence of explosive gases without requiring a costly sealed housing. This is a highly desirable feature for such wireless adapters. On the other hand, the regulations on IS limit the energy that can be accidentally delivered by the electronics [3][4][5]. One of the consequences is that only relatively small capacitors are directly allowed. For example, if the voltage on the capacitors is limited to, e.g. 5V, the sum of all capacitors should not exceed 100µF for group IIC apparatuses (devices that are allowed to operate with the most volatile gases [3]). There are techniques to limit the energy that can be delivered by capacitors: add a serial resistor to limit the energy or impede the energy to flow back to the hazardous area by means of barrier diodes. Unfortunately, the first technique implies important resistive losses while the second technique adds a severe voltage drop.

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[1] The full adapter also consists additionally of a radio part that is powered by the DC/DC converter and that digitally communicates with the HART modem; the wireless modem is depicted in Figure 2 for the sake of completeness but is not described in this paper.
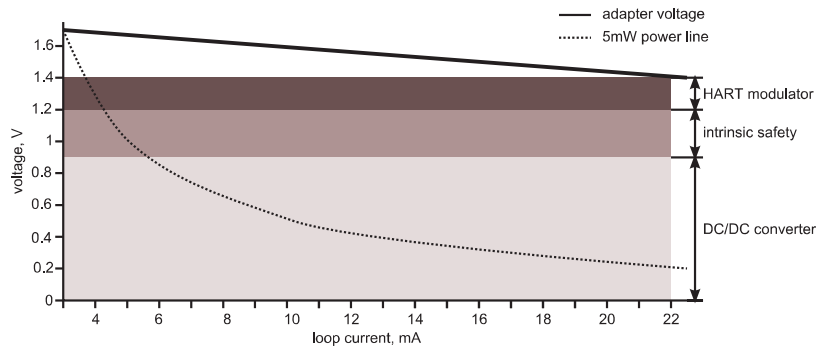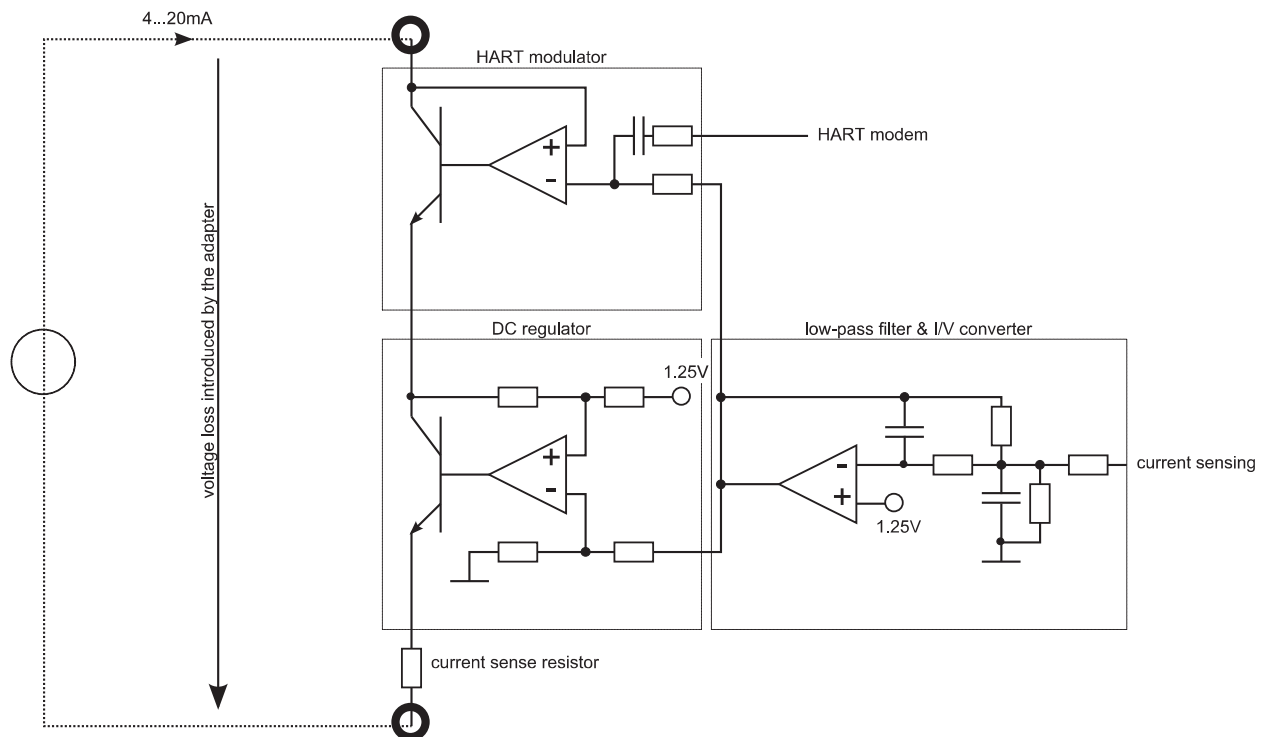
Figure 3, voltage drop created by the adapter

Figure 4, voltage modulator driving and analogue signal processing

3.   Adaptive voltage drop regulation

The central idea of "adaptive voltage drop regulation" is to update the voltage loss created by the adapter according to the current flowing into the loop. Because the current is defined by the signalling device and the adapter needs a constant power to operate (about 5mW), the adapter requires less voltage to operate at higher signalling current than at lower current. Additionally, the resistive voltage loss introduced by the wiring is maximal at higher current. The voltage available to the field device is minimal at 20mA and maximal at 4mA. In practice the wiring is often close to the maximal allowed length in the sense that the voltage supplying the field device is close to the lower limit accepted by the field device. It is thus of advantage, and possible, to reduce the voltage drop created by the adapter at higher signalling current.

The voltage drop created by the wireless adapter is larger at low current than at higher current as shown in Figure 3. Not only does the minimum voltage drop created by the adapter depend on the signalling current, but it also depends on the minimum input voltage required by the DC/DC converter. In our case, the latter is about 0.9V to which 300mV have to be added to account for the losses introduced by the intrinsic safety mechanisms and 200mV for that of the HART modulation stage.

An overview of the voltage drop adaptation implementation is shown in Figure 4. It is based on analogue processing of the signalling current. First, the analogue current is sensed on a low-impedance resistor (1.1Ω to minimise voltage loss) and amplified with a single-ended two-stage amplifier that achieves a trans-impedance gain of 130V/A. Second, the voltage image of the current is filtered with a second order

low-pass filter based on Sallen-Key topology with a 3dB point at 10Hz. Third, the smoothed image of the current is converted into a voltage drop "set value" using an affine transformation to convert the signalling current into the required voltage drop (I/V transformation). Fourth, the voltage drop is regulated using a voltage shunt transistor by the HART modulator and, at the same time, a DC voltage is similarly generated for the step-up converter. The low-pass filter and subsequent stages are detailed in Figure 4. The low-pass filter I/V transformation are done using the same operational amplifier; the affine transformation results in the set value V_{SET} = 1.46·1.25V - 0.123·V_I. The set value is then directly mirrored on the adapter voltage drop while the DC regulator slightly updates it as follows V_{DC} = 1.02·V_{SET} - 281mV; the 281mV accounts for the DC voltage needed by the HART modulator. This implies that the voltage drop incurred by the adapter is about 1.4V at 22mA and about 1.7V at 3.6mA. Monte-Carlo simulations show that those values are stable at better than ±3% if 1%-precise resistors and sub-10mV input offset voltage operational amplifiers (e.g. OPA349) are used.

4.   Low voltage reverse-current Blocking Barrier

To comply with IS standards, large capacitors have to be enclosed within a protecting enclosure (e.g. coating or potting) and connected through a reverse-current blocking barrier to the outside electronics [3]. This limits energy, both thermal and electrical, that could be transferred, in case of failure, from the capacitors to parts outside the protecting enclosure. The smoothing capacitor before the DC/DC converter, Figure 2, is too large according to the standards and a barrier is needed. Unfortunately, conventional solutions, such as diode-based circuits, induce a large voltage loss. Complex circuits, such as integrated circuits, are not allowed by certification bodies because the faults are then difficult to analyse and the protection also has to operate without power supply. For this reason, we propose a new zero-power barrier but with better performances than the diode-based solution.

We now consider state-of-the-art IS protection circuits that enable the current to flow in one direction (forward mode) while blocking the current in the other direction (reverse mode) [4]. The standard approach consists in using silicon diodes connected in series [5][6]. In some world regions, two diodes are enough while in others regions, three diodes are mandatory. Typically, the voltage drop of a single silicon diode is about 0.6V in forward mode at room temperature. To minimise voltage losses, Schottky diodes are instead used. The total voltage drop caused by three series Schottky diodes is around 0.5V at room temperature. However, when the temperature decreases there are fewer charge carriers and the voltage drop increases for a given current. In this case, the voltage loss can grow up to 1V at -40°C.

The proposed solution is shown (for three protection stages) in Figure 5. In forward mode (U_I>U_O), only the lower transistors and resistors define the behaviour of the protection circuit. Indeed, the upper transistors are reverse-biased and thus non-conducting. The lower transistors are forward-biased in such a way that they are in forward-active mode and saturated (their collector-emitter voltage is minimal). In this case, the total voltage drop caused by the three transistors is very low at any temperature. Since the transistors are saturated, the needed basis current is much higher than for normal forward-active mode. This implies that a non-negligible amount of the emitter current goes into the transistor basis. In reverse mode (U_O>U_I and U_O>0.6V), the upper transistors are forward-biased and thus conducting. Their purpose is to render the lower transistors group non-conducting by reverse-biasing them. Note that this is needed because bipolar transistors are fairly symmetrical. Indeed, collector and emitter can be inverted and the transistor still works as a transistor, albeit with worse characteristics. This implies that a protection circuit composed of only of the lower transistors would not fully block the current.

For U_I=1.5V and I_I=4mA, we measure at -40°C a forward mode voltage loss of about 0.78V for three series Schottky diodes (ZHCS1006). The power efficiency is thus about 48%. For the proposed transistors solution (based on FMMT717 and for lower resistors with value 18kΩ), we measure under the same conditions a forward mode voltage loss of about 193mV and current loss of about 69μA. The power efficiency is thus about 85%, which is much better than for the diodes. A more detailed discussion and analysis of the transistor-based blocking barrier can be found in [7].

Future work is for example to enable the transistor barrier function for input voltage below 1V. Indeed it is at the moment difficult to bias the bipolar transistor so that it is in saturation mode, at all temperature and without spending too much basis current, for such low input voltage.
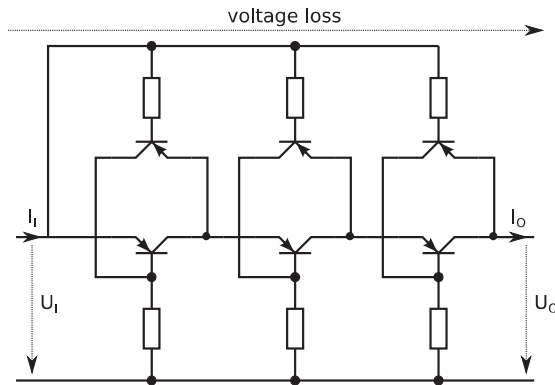
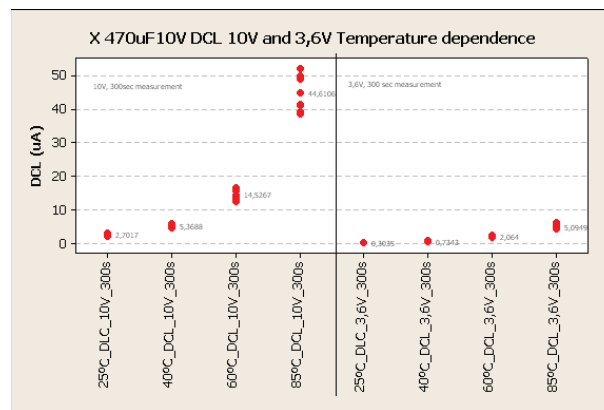**Figure 5, proposed novel reverse current blocking barrier**

Figure 6, leakage measurements on six 470µF capacitors, courtesy of Kemet

5.   Capacitors bank leakage optimisation

The wireless HART chip requires more peak power than can be extracted from the 4…20mA loop (e.g. up to 100mW during as long as 30ms). A large capacitive buffer of 6mF is used to average out peak power. Unfortunately, the buffer presents a leakage current up to 600uA at +85°C. Unfortunately, discussions with capacitor suppliers showed that leakage current is not a primary optimisation target in the solid electrolytic capacitors market (contrary to ESR or capacitance). To lower leakage, a solution is to use tantalum capacitors with an optimal ratio between rated and used voltages [8].

An important problem with such a large capacitive bank is the large leakage it incurs. Indeed, only electrolytic capacitors could achieve 6mF within a reasonable footprint. Some special aluminium electrolytic capacitors exhibit very low leakage current but are ruled out because of intrinsic safety requirements (no liquid electrolyte is permitted [3]). The remaining standard choice is solid electrolyte and thus (mainly) tantalum-based and Niobium-oxide capacitors.

For tantalum capacitors, a study has shown that the smallest leakage is obtained by using capacitor running at about 30-40% of the rated voltage [8]. In the adapter case, the maximum voltage is 3V, which means that the capacitor should be rated for about 10V. For this reason, the capacitive bank could be formed by twelve 470µF/10V capacitors. More precisely, let us consider the B45197A2477K509 from Kemet [9] because we had access to informative leakage measurements for that type. The measurements show that typical leakage currents are much lower than those documented in the datasheets.

Using derating graphs [9], the leakage of these capacitors is at most 8.5µA per capacitor (p.c.) at 25°C; furthermore it can be multiplied by up to five at 85°C. On the other hand, the measurements done by Kemet show that actual values are much lower as reported in Figure 6. For example, the leakage current at 25°C is 0.3µA p.c. and increases to 5.1 µA p.c. at 85°C. These results thus support the ones reported previously in [8] by another capacitor supplier. Future work is however necessary to confirm this rule of thumb at operating temperatures other than 25°C.
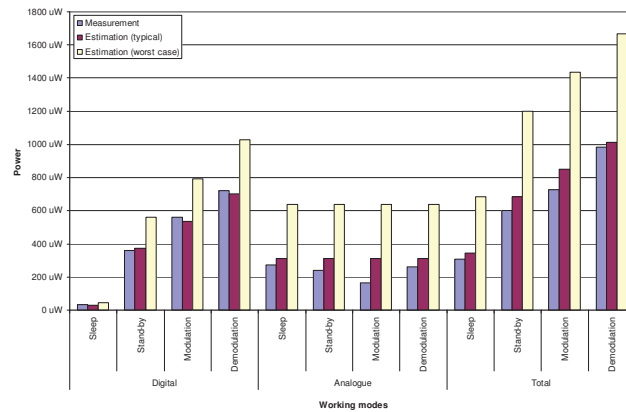
Figure 7, power consumption comparison between measurements and estimations

6. Power consumption results

The electronics were designed using an iterative approach to optimally distribute the power budget according to the different operation modes (stand-by, demodulation, modulation) and device structure (analogue, digital). The power consumption estimation is done using a simple approach as detailed thereafter. For the analogue electronics, the quiescent currents $I_{Q,i}$ of the used analogue integrated circuits are found in the corresponding datasheets; additionally every resistor value R_i is used. The analogue power consumption estimate is then given by $V_{cc} \cdot \Sigma_i I_{Q,i} + V_{cc}^2 \cdot \Sigma_j R_j^{-1}$ where V_{cc} is the supply voltage; the estimate is the same for all operation modes. For the digital electronics, the fraction of time α_{mode} that the microcontroller spends in active state is roughly estimated for each operation mode (0%, 50% and 25% for stand-by, demodulation and modulation respectively). The digital electronics power consumption is then given, for a certain mode, by $V_{cc} \cdot I_{active} \cdot \alpha_{mode} + V_{cc} \cdot I_{sleep} \cdot (1 - \alpha_{mode})$ where I_{active} is the microcontroller active-mode current and I_{sleep} is the microcontroller sleep-mode current; both current values include the current of. This enables an early and easy estimation of the power consumption of each important part under different conditions. It is then possible to optimise the relevant sub-circuit in any operating mode. For example, the final estimated power consumptions are given in Figure 7 where typical / maximal quiescent currents are used to get typical / worst case power consumption. It is shown that further reduction of the maximal overall power consumption is obtained by optimising the digital electronics in demodulation mode. For example, this could be performed by replacing digital by analogue demodulation; the power consumption of the demodulation is reduced by a factor ten [10]. Additionally, Figure 7 shows power consumption measurement results. It can be observed that for the digital electronics the typical estimates are rather close to the measured values. On the other hand, the typical estimates for analogue electronics are comparatively slightly overestimated; this is because we assumed, to simplify the estimation step, that all resistors see the full supply voltage, i.e. 3V.

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