Cost Modeling of Radio Sensor Systems for Industrial Applications

Dr.-Ing. Dr. rer. oec. Niedermayer, Michael
Fraunhofer Institute for Reliability and Microintegration
Gustav-Meyer-Allee 25, D-13355 Berlin

1. Introduction

The implementation of wireless sensor networks in complex machinery and plants paves the way for advanced concepts in condition monitoring and remote maintenance. The smallest irregularities on rolling bearings and gears can be recognized by sensitive vibration sensors to detect the damage status. Radio sensor systems provide cost-efficient solutions in a broad range of industrial applications ranging from process monitoring to material logistics. Radio sensor systems exhibit a lot of design trade-offs regarding system behavior, hardware architecture and fabrication technology.
Conventional design flows typically only allow cost evaluations at the end of the development process after component geometries and the technology choices have been fully specified, whereas an efficient cost minimization requires a systematic approach which guides the designer into optimizing the cost-relevant elements during the whole design process. Hence, our design methodology for cost-efficient radio sensor systems is based on cost models.
Scientific publications usually avoid a discussion about the cost dependencies on the assumption that this is beneficial for the objectivity, rigorousness and permanency of the contents [1]. To permit a cost discussion on a more general basis, our work explores the cost dependencies of the system components for wireless sensor networks on a more general base. This results in cost models and metrics that allow a better assessment of the various structural and technological implementation options. The corresponding data was derived from several research projects about the economics of micro system technologies.Many cost categories exist for the allocation of expenditures. Relevant costs for sensor nodes include [2]:

- Non-recurring design and development costs,
- Capital costs, tooling costs, learning curves,
- Recurring fabrication and assembly costs,
- Repair and rework costs, testing costs,
- Installation and maintenance costs.

For our analyses, we distinguish direct costs (DC) from indirect costs (IDC). The direct costs can be associated with a single sensor node, such as component costs and process costs during its production. All other expenditures form the indirect costs, which have to be broken down into the number of produced sensor nodes. The more devices required, the lower the fraction of indirect costs per unit. The indirect costs are often further divided into the non-recurring expenditures (NRE) and costs caused by the yield loss [3]. The indirect costs can be easily assigned to one specific application whenever the costs are only related to a unique product. Usually, a portion of the indirect costs has to be allocated over several applications. This cost distribution also depends on the expectation of the future business. The indirect costs should be considered separately due to that subjective degree of freedom. Distinguishing between direct and indirect costs is common practice, however the mapping of individual cost items to those categories is often varied depending on the objective and the degrees of freedom during the cost optimization process [4], [5], [6].
Furthermore, we introduce the categorization into functional components as well as integration elements in order to derive cost metrics for the system functionality ($ per function). The cost parameters based on functional components can be used as optimization criteria during the network and architecture design. However, the cost metrics regarding the integration elements are especially relevant for the physical design and the selection of fabrication sequences. With the knowledge of the cost fundamentals of functional components and integration elements, the cost drivers can be more easily identified in the conception phase. During later product development, the cost optimization will require further cost inquiries and process analyses for a refinement of the cost models [7]. Thus, the accuracy of cost estimations gradually increases in order to evaluate the different implementation options of wireless sensor nodes. The individual cost aspects of component technologies as well as integration technologies will be considered in the following subsections in order to structure the costs of wireless sensor nodes. Whenever possible, rough cost ranges in the currency Euro (€) are given.

2. Direct Cost of Functional Components

Besides sensors and actuators, radio sensor nodes provide advanced functionality regarding data processing and communication which is basically realized by the semiconductor technologies. In addition to the annual cost reduction per chip of 30% [8], the ongoing technological reduction of the feature size also allows an improved energy efficiency. Hence, modern IC technologies permit further cost reduction resulting from lower power consumption. These cost savings for ICs with small feature sizes can only be realized for large quantities, because the modern IC technologies require increasing manufacturing costs per wafer due to the higher process complexity and the equipment costs. The most commonly used cost metric is related to the production costs per chip area.

While cost per chip area and minimum feature size are a powerful metric for IC cost analyses, the range of sensor costs is by far broader in dependence of measurement type and accuracy. The main reasons for this are larger process diversity and varying sensor requirements. Hence, on-chip integrated temperature sensors with an accuracy of two degrees Kelvin cost a fraction of one cent, while more precise MEMS-sensors are often priced above 1€. For specific niche applications, sensor costs of several hundred dollars are not unusual, e.g. for 3D-acceleration sensors with extreme shock resistance.

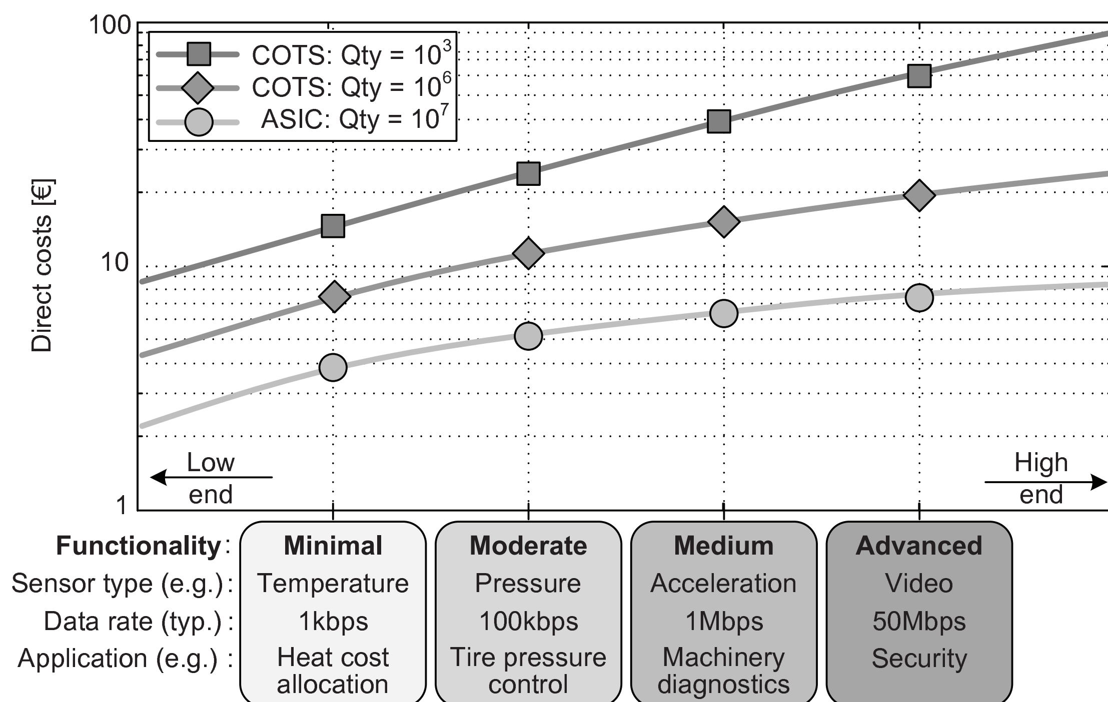

Figure 1: Direct Costs for Functional Components of Wireless Sensor Nodes [9]

Based on quotes for components off-the shelf (COTS) in large quantities, Figure 1 lists cost ranges of radio sensor nodes in dependence of the required functionality. The direct costs for the exclusive use of COTS are also slightly higher for large quantities because the manufacturers have already distributed their indirect costs into their product prices. An in-house development allows lower direct costs, because our approach takes the later discussed indirect costs separately into account. The direct costs of the functional components are increasing with functionality. The invoice for materials can also reach the region of several hundred dollars if additive functionality or restrictions – such as extended temperature range, higher sensor accuracy, very large memory and fast sampling frequencies – are required. The resulting direct costs of the functional components determine the lower cost bound for a given functionality.

3. Direct Cost of Integration Elements

Besides the direct costs for each functional component, additional expenditures are necessary for the realization of the entire radio sensor system. The costs of module integration include all expenditures for the electrical and mechanical interconnections of the functional components. This includes the packaging of one or more functional components as well as the module assembly on carrier substrates. Ideally, the integration elements can be considered entirely dissociatedly from the system functionality. In practice, the isolated view cannot be maintained during the latter stages of design implementation because

parasitic effects have to be taken into account, for instance thermo-mechanical stress of sensor interconnects or electromagnetic crosstalk in adjacent connections. The direct costs for the integration of smart micro sensors typically range between one and five dollars, usually 10-50 percent of direct costs for the functional components. For special requirements, the cost fraction can reach as much as 90 percent of the total costs if the application requires high precision or reliable operation in harsh environments. The following cost margins are based on the work of [1], [10] and [11] in conjunction with up-dated values by own quotes.
Figure 2a gives an overview of direct costs of substrate technologies in dependence of the wiring capacity. Conventional printed wiring boards (PWB) provide the lowest costs per area. The costs start from 0,005€ per cm² and metal layer, as long as the interconnection pitch is below 250 microns. The further development of PWB, known as sequential build-up (SBU), costs roughly 0,10€ per cm². These substrates allow the processing of bare dies due to an acceptable interconnection pitch of 100 microns. SBU-substrates can provide a cost-optimal solution, if all functional components of a smart micro system are available in very small dimensions to reach very high integration densities. The cost savings result from the reduced substrate area which is required to interconnect all functional components. There are even more expensive substrate variants to improve parameters such as radio frequency loss or temperature stability. In particular, the class of thin film substrates with a wiring pitch below 50 microns bridges the gap between IC technologies. The cost of SBU, ceramic and thin film substrates can be significantly higher if processes for embedding of dies and passives are included. The corresponding cost increase is recouped for larger quantities whenever cost reductions can be realized due to smaller substrates or higher shock robustness.

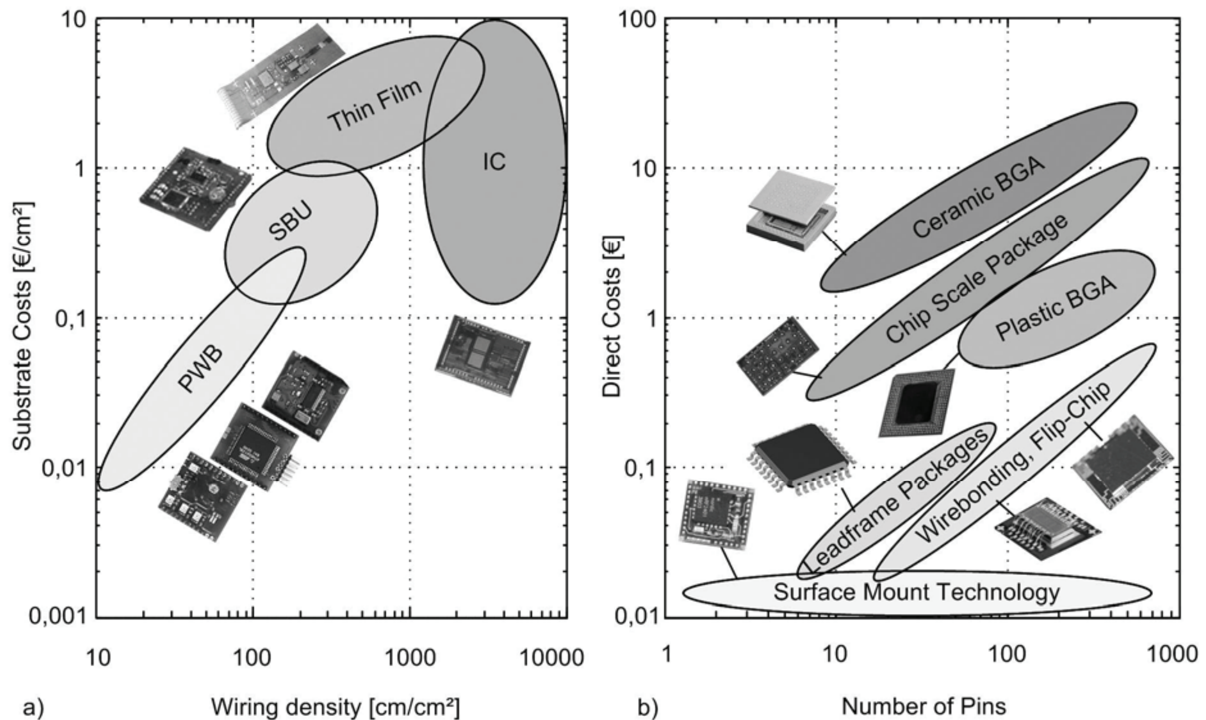

Figure 2: a) Direct Costs of Substrates; b) Cost per Pin for IC Interconnection and Packages

Since dies can require a pad pitch of below 100 microns, the use of low-cost printed wiring boards requires packaged micro chip to have an enlarged interconnection pitch. Plastic packages based on lead frames provide the most inexpensive solution for single chip packaging with costs of approximately $0,05 per pin. The pins are arranged peripherally. Examples are the Thin Small-Outline Package (TSOP), the Thin Quad Flat Package (TQFP), and the Micro Lead Frame Package (MLF). Above 40 pins, packages with an area contact arrangement such as ball grid arrays (BGA) allow more dense interconnects with a pitch of 1 millimeter or larger. A multi-layer substrate is used instead of the lead frame. The costs for these packaging options start from 0,03€ per pin plus 0,15€ basis costs in case a combination of SBU, wire bonding (WB) and plastic encapsulation is to be applied. Instead of wire bonding for chip interconnection, the use of the flip chip (FC) method allows for shorter line lengths with less inductance for an additional 0,03€ per pin. Considerably more expensive are hermetically sealed ceramic packages with costs of approximately 0,03€ per pin plus 0,40€ overhead. Chip Scale Packages (CSP) with array

grids of below 1mm reach cost dimensions above the expenditures for plastic BGA with flip chip interconnects.
The costs for the packaging of individual chips can be spared by directly attaching the bare dies onto a module substrate. The corresponding expenses start from 0,007€ per pin for direct chip interconnection by wire bonding or by the flip chip method. Up to 0,03€ per pin becomes necessary for flip chip with advanced requirements. This is far more expensive compared to the costs of the surface mount technology (SMT) for soldering packaged components, which amount to below 0,01€ per module. The cost differences mainly result from higher equipment costs. Figure 2b summarizes the costs of single chip packages and chip interconnection technologies. The cost of multi-chip packages can be roughly estimated by adding the costs of the equivalent combination of the single chip package and the applied chip interconnection technologies [7].

4. Indirect Costs

The indirect costs of the functional components significantly depend on the availability of COTS and their costs. Expenditures for a component development have to be considered if COTS are not available or if significant savings of direct cost can be realized. The development costs are usually a very significant fraction of the total costs, in particular for radio sensor nodes in moderate fabrication quantities. Additional development effort is often a powerful measure of cost optimization by reducing direct costs of components. However, this requires increased indirect costs for the development which can be especially advantageous if the cost portions for component developments can be distributed over several applications. The normally higher degree of uncertainty regarding the time schedule makes the cost of new developments difficult to predict.

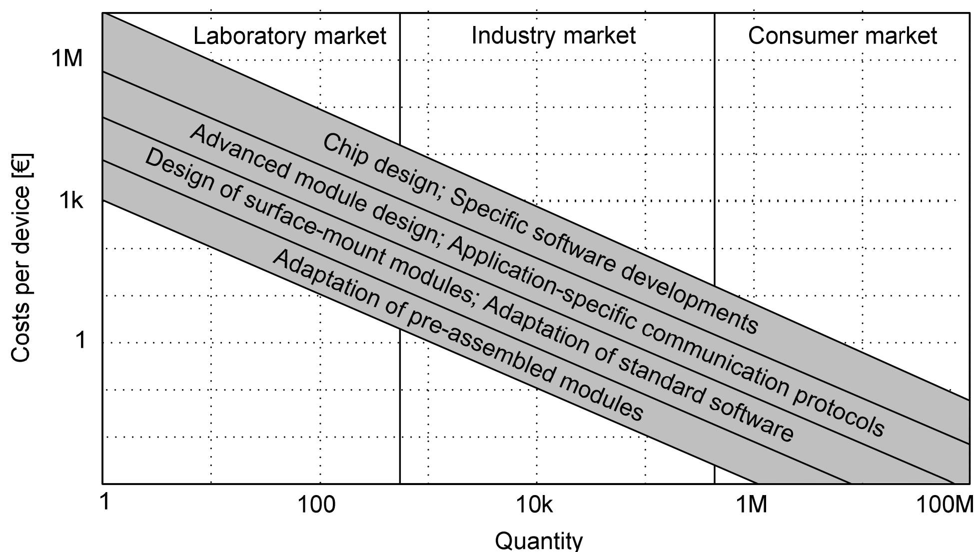

Figure 3: The Influence of Indirect Costs

The constructive cost model COCOMO II [9] is well-suited for assessment of the development effort. Hence, the non-recurring expenditures are estimated based on the required team size and necessary lines of code (LOC) depending on whether high-level source code or hardware related driver software is to be implemented. Generally, the costs for development and equipment vary on a large scale. Figure 3 illustrates the cost fractions of several indirect costs for smart micro sensors.

4. Cost Optimization of Radio Sensor Nodes

Our design approach requires a regular refinement of the cost model for a specific smart micro system during the whole development process. We have implemented a design environment in order to provide up-to-date cost metrics for different design domains [9]. The concept is illustrated in Figure 4. Libraries are currently created which will ease the entry of the cost data for the different functional components and integration elements. Specific program modules have been implemented for cost estimation of selected system components, process flows and product development activities. The design environment is able to guide the user during the development process by identifying the cost-driving trade-offs. Since knowledge of previous projects is available in the libraries, the user can load detailed cost models and adjust the corresponding parameters.

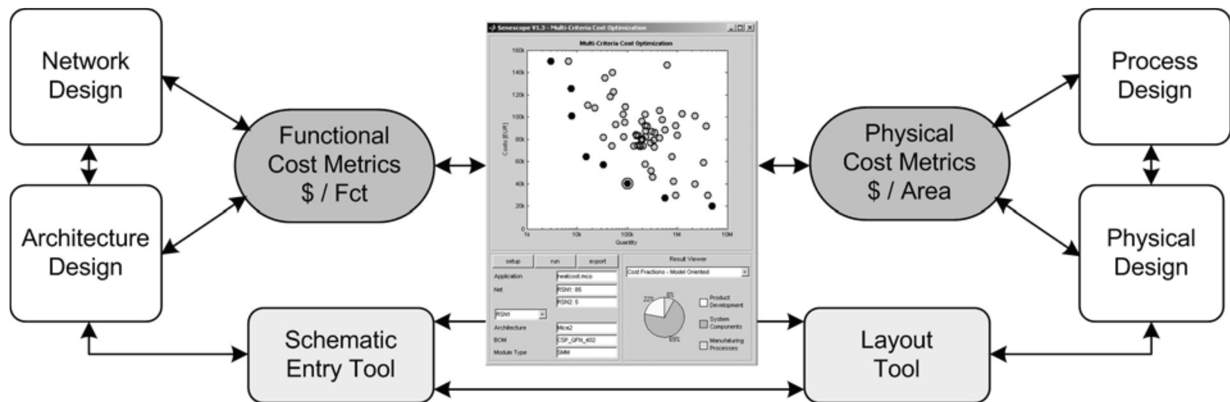

Figure 4: Concept of the Design Environment for Cost Optimization of Radio Sensor Nodes

Our approach will change the design of radio sensor nodes by identifying the cost driving elements in order to adjust the development focus of the further optimization steps. Thereby, the level of detail must be balanced against the complexity of the cost models which guide the design flow. Initially, a simplified cost structure based on functional components and integration elements is assumed. During later stages of design implementation, more detailed analyses result in more accurate predictions of the cost driving elements. The model refinement is only necessary for the significant cost fractions. In order to reduce the effort for model parameterization and to improve the computation efficiency, three levels of cost representation are supported by the cost modeling editor for the system components (Table 1).

Table 1: Levels of Model Granularity

Representation	Remark	Example
Fixed Cost	Fixed cost values in case of marginal significance or variance	e.g. C_1 = 0.79 [EUR]
Cost Diagram	Data entry of characteristic curves for the interpolation of cost parameters	e.g. cost/quantity chart N = [1, 10, 100, 1000]; C_1= [15.5, 11.3, 9.4, 7.2]
Process Flow	Activity based cost models by categorizing process costs into cost for labor C_L, tools C_T, material C_M, and capital C_C	e.g. fabrication sequence P1 (Wafer Preparation): $C_{P1} = C_{L1}+C_{T1}+C_{M1}+C_{C1}$ P2 (Wafer Test): $C_{P2} = C_{L2}+C_{T2}+C_{M2}+C_{C2}$ $\rightarrow C_1 = C_{P1}+C_{P2} + \ldots$

Besides the declaration of fixed cost values, the entry of so-called cost diagrams are supported to specify the known component costs in conjunction with some reference parameters (e.g. order quantity N or layer number L). The component costs will be interpolated if the value of a parameter is different from that specified in the cost diagram. Otherwise the cost diagrams serve as look-up table. For a more detailed cost modeling, the cost parameters are extracted from activity based process flows. The corresponding cost models can be created and modified by the editor for manufacturing processes. In that case, the cost of a system component results from the fabrication sequence with the lowest process costs. The editor for the process cost models follows the approach of the cost optimization tool Savansys [12].

5. Application

Condition monitoring of industrial machinery was chosen as one very promising application scenario. Thereby, the wireless sensor nodes are to detect vibration magnitudes in order to trigger maintenance intervals in case of abnormal vibrations. A MEMS-based acceleration-sensor with moderated data processing and network functionality was analyzed regarding architectural implementation variants and technological options.

The objective was to design a cost efficient sensor node for an assumed quantity of 50k per year. The fully functional design study is illustrated on Figure 5a. The CC430 from Texas Instruments – a 16-bit-microcontroller and radio transceiver integrated on a single chip – was used to minimize the direct costs of the functional components. The indirect costs of 50k€ include the adaption of the sensor node software at a 20% fraction, the hardware and software costs for the user interface at 35% as well as the remaining 45% for the SBU design. The moderate lot size of 50k does not justify any more development effort for further reduction of direct costs. (Figure 5b).

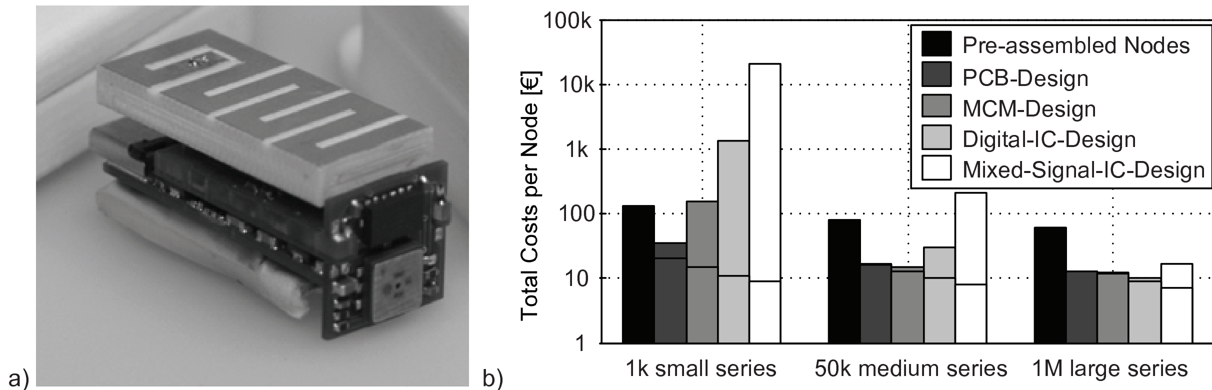

Figure 5: a) Design Study of a Condition Monitoring Radio Sensor; b) Resulting Costs per Device

Pre-assembled modules, such as the MicaZ-nodes from Crossbow, would be the best solution for small quantities in the range of 1k. Thereby, the additional direct cost for the larger memory is recouped by the advantage of the accelerated software programming. In excess of a million devices, an ASIC-development is recommendable reaching costs of below 10€ per node. Such sensor nodes allow for the implemention of a condition-based maintenance. If the downtime of machinery inevitably leads to considerable costs, the measured data can also be evaluated from remote locations.

6. Conclusion and Future Work

The design of cost-efficient radio system systems requires analyses of various trade-offs regarding system functionality, component selection, and manufacturing technologies. The implemented design environment supports a cost-driven selection of sensor node architectures and fabrication processes.The results are of fundamental importance, since many industrial applications of radio sensors are not marketable until a specific cost level has been reached.
The currently implemented software prototype for the cost modeling of sensor nodes will be further developed to accelerate the cost optimization of sensor networks, especially during the phase of design conception. Furthermore, the underlying libraries will be enhanced by a larger number of models for cost estimation of system components, manufacturing processes and product development. This requires a regular update by empirical data from market studies to improve accuracy of the cost calculations.

7. References

[1] Messner, G., and Smit, W.: “Equations for selection of cost-efficient interconnection designs,” Proc. 41st Electronic Components and Technology Conf., San Diego, CA, 1992.

[2] Sandborn, P., Conceptual Design of Multichip Modules and Systems, Dordrecht, Netherlands: Kluwer Academic Publishers, 1994.

[3] Scheffler, M.: "Cost vs. Quality Trade-off for High-Density Packaging of Electronic Systems", Ph.D. Thesis, ETH-Zurich, Switzerland, 2001.

[4] Ng, L., “MCM Package Selection: Cost Issues.” In Multichip Modules - Technologies and Alternatives: The Basics, pp. 133–164, D. A. Doane and P. D. Franzon (eds.), New York, NY: Van Nostrand Reinhold, 1993.

[5] Alexander, M., K. Srihari, and C. Emerson, “Manufacturing Cost Analysis of Surface Mount PCB Design,” The Journal of the Institute of Circuit Technology, Vol. 20, No.4, 1994, pp. 28–32.

[6] Sandborn, P., M. Abadir, and C. Murphy, “The Tradeoff Between Peripheral and Area Array Bonding of Components in Multichip Modules,”, IEEE Trans. CPMT Part A, Vol. 17, No. 2, 1994.

[7] Niedermayer, M., et al.: "Cost-Driven Design of Smart Micro Systems", 2st Int. Conf. on Smart Systems Integration 2008, Barcelona, Spain, 2008.

[8] Goodall, R., et al.: "Long-Term Productivity Mechanisms of The Semiconductor Industry" Semiconductor Silicon, Vol. 2, 2002.

[9] Niedermayer, M., et al.: "SENESCOPE: A Design Tool for Cost Optimization of Wireless Sensor Nodes", Proc. of IPSN Track on Sensor Platform, Tools and Design Methods for Networked Embedded Systems, San Francisco, CA, 2009.

[10] E. Bogatin, "Roadmaps of Packaging Technology," Integrated Circuit Engineering Corporation, Scottsdale, AR, 1997.

[11] S. W. Jones: "IC Cost Model", IC Knowlegde LLC, Georgetown, MA, 2010.

[12] Palesko, C.: "Activity based cost modeling for embedded passives", Proceedings of IPC Conference on Em-bedded Passives, Northbrook, IL, 2003.