Smart Sensor Systems - Packaging Technologies for Multi-Sensory Consumer Applications

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Advanced silicon technologies offer the possibility of integrating hundreds of millions of transistors in a single electronic component such as a microprocessor. Experts predict that the increase of components per chip will follow the well known “Moore’s law” in the next decade, too. “Microelectronics” will become “Nanoelectronics”. This trend can be characterized by “More Moore”. If electronic signal and data processing systems are focused, nanoelectronic components will be very cost efficient due to larger wafer sizes and a high degree of miniaturization (System-on-Chip). But future multifunctional systems require not only more signal and data processing power but also require interfaces to the human sensory organs and altogether functions for an interaction with the environment. Besides these, antennas, components for optical signals and data transmission as well as functions for energy conversion and storage are also needed.

However, for these future multifunctional technologies in most cases the cost efficient nanoelectronic standard technologies cannot be applied. Non-electronic and often radiofrequency functions require alternative materials and special processes. This additional process steps often reduce the yield or require special process developments which result in a tremendous cost increase. Therefore pure “System on Chip (SoC)” solutions will be supplemented by “More than Moore” solutions. “More than Moore” uses standard technologies for the realization of multifunctional system technologies based on devices realized by heterogeneous processes.

Both “More Moore” as well as “More Than Moore” solutions are aiming at single component solutions provided to the customer. As far as technical and economical feasible these “System on Chip” or as well monolithically integrated “More Than Moore” solutions will be chosen.
But more and more applications are asking for specific application specific integration technologies or the flexible integration of highly complex systems containing digital and non-electronic functions. Therefore the future of Nanoelectronics will see a combination of ‘More Moore’ and ‘More than Moore’ components, combined in one package (‘System-in-Package’ or SiP). With such a SiP solution, the application benefits from a comparable level of miniaturization to that achievable with a “System on Chip” (More Moore) solution, from the enhanced functionality of “More than More” solutions and it also benefits from having each part of the system fabricated in an optimum process technology.

One of the reasons “Heterogeneous Integration” (HSI) concepts are gaining importance is the lower cost and risk assessment compared to “System on Chip” and monolithically integrated “More than Moore” solutions. Further advantages include their shorter time to market cycle and a high degree of flexibility. This high flexibility of “Heterogeneous Integration” certainly offers the possibility to integrate “System on Chip” as well as “More

than Moore” solutions, for example for subsystems. The quota of “System on Chip” and “More than Moore” solutions in such a Heterointegrated System depends strongly on cost issues per component and also the demands of the final product.

The present status of system integration is still dominated by single-chip packaging, with the few stacked-die SiP solutions being implemented mainly using wire bonding. Their design and implementation uses advanced substrate board, so called “High Density Interconnect”(HDI) multi-layer boards. But, unlike the integrated circuit industry, where electrical, thermal and mechanical characterization is allocated to the complete design, the chips, package and board in such heterogeneous SiP solutions are still designed separately and do not share a common ground.

This currently applied approach will not be sufficient to meet the future integration requirements of advanced SiP solutions. The very high level of miniaturization and extreme reliability required in future SiPs will mean that issues such as thermal and mechanical stress management will need to take into account everything between the point at which heat is generated and the outside of the package. It will be further complicated by integration of special functions into the package, such as sensors, actuators, RF interfaces or power supply components, which may be especially sensitive to heat, stress etc. In addition the application environment in which the SiP will ultimately be used will also need to be taken into account.

To meet these challenges, new methodologies and architectures will have to be developed. To reach the required level of miniaturization, it will e.g. be necessary to develop advanced assembly and handling technologies for thin wafers and chips. The integration of nano-ICs, sensor chips, actuator components, passives and displays into 3-D architectures will require the development of new design methodologies as well as reliable ultra-thin metallic interconnect technologies. New low-cost solutions for heat dissipation and thermal and RF shielding will have to be investigated and improved thermal interfaces are required to provide adequate thermal management.

Especially for the consumer market additional efforts need to be made regarding meeting the cost targets for these applications. Though the device reliability is often limited for consumer applications, the cost & manufacturing issues need to be handled appropriately. An example for this can be the INFON-Project, where a consortium of Infineon, SAT, Peiker and Fraunhofer IZM have developed a packaging technology for a silicon microphone, that was both simple and thus cost effective and additionally well suited for consumer and also automotive use. Technologies chosen were stress decoupling die attach for the sensitive MEMS-microphone and mature Chip-on-Board interconnection technology for MEMS interconnection and ASIC assembly. In Figure 1 a schematic and test samples of such packages are depicted. [1]

Future applications will need the even more miniaturized integration of a larger amount of devices, where more advanced technologies as substrate and mold module embedding, 2D and 3D interconnect redistribution and also device stacking will be applied – and thus need to be investigated. In addition, improvements in design and simulation methodologies, test strategies and reliability modelling are required. This research work has to be accomplished through the common effort of technology users and technology and equipment providers, as well as the appropriate European research institutes. [2; 3; 4]

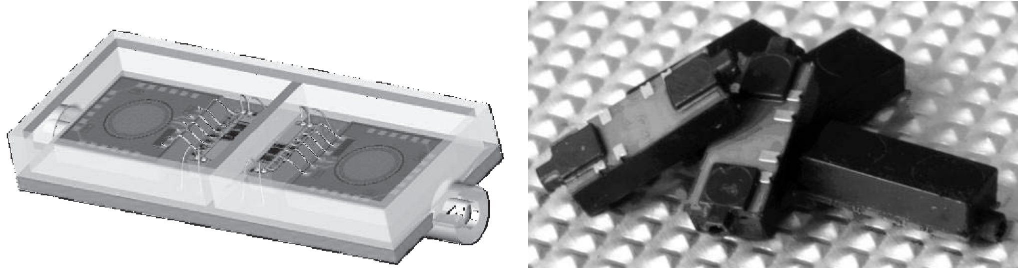

Figure 1: Schematic of a Si-microphone array package (left) and Si-microphone array package realized within InFON (right)

Based on the initial success of these approaches, several companies have now started to work more closely on similar concepts, integrating multiple components from different manufacturing processes (also including SoC and monolithic More than Moore devices) into subminiature packages with very high functional density per volume. The shift from the paradigm "function per area" towards "function per volume" is also important to assess the future impact of SiP´s as with planar technology alone that step cannot be made.

Conclusion:

The advent of monolithically integrated systems "More than Moore" leveraging nanoscale technology for sensors and RF systems as well as the growing maturity of System on Chip (SoC) solutions have increased the function per area significantly. Packaging technology now enables to use these devices in a maximum level of integration, enabling also the use of the third dimension to a paradigm shift towards function per volume.

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