MEMS Capacitive Sensor Interfaces: Can we Solve the Challenge?

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Introduction

It is well known that integrated capacitive mechanical sensors offer much higher potentials than their piezo-resistive counterparts as far as sensitivity, temperature behaviour, stability and power consumption are concerned [1]. However, their adoption in regular applications is still moderate, despite these excellent characteristics. One reason is clear : inherently, it is not wise to miniaturize such sensors. The concept is in fact not very compatible with the basics of MEMS, i.e. : the parasitics become dominant when reducing the dimensions ! The exploitation of miniaturized capacitive sensors is often inhibited by the presence of parasitic effects, such as environmental noise, parasitic capacitances and leakage resistors. These effects are much less pronounced for piezoresistive devices. The mentioned parasitic effects are of a fundamental nature and are inherently related to miniaturization in the case of a capacitive device. Down scaling of the sensor dimensions implies down scaling of the active capacitance values (to the second power !). Thus, full integration implies active sensing capacitances that get as low as a few fF only. Hence, high output impedances and noise sensitivity cannot be avoided and the effects of stray capacitances become more dominating. The only way to cope with these difficulties is to incorporate a dedicated readout circuit in close proximity of the sensor, i.e. in the sensor package itself.

This paper has a dual approach to this problem : at first, it will highlight techniques to cancel out such parasitic effects, and secondly, it will focus on a impoved low power offset cancellation solution.

Capacitive pressure sensors

Figure 1 shows a typical layout and cross-section of a capacitive pressure sensor. The sensor basically consist of a glass/silicon sandwich with overall dimensions of 2.2 x 3.5 x 0.8 mm. Starting material is a p-type double-side polished silicon wafer with a n-type epitaxial layer.
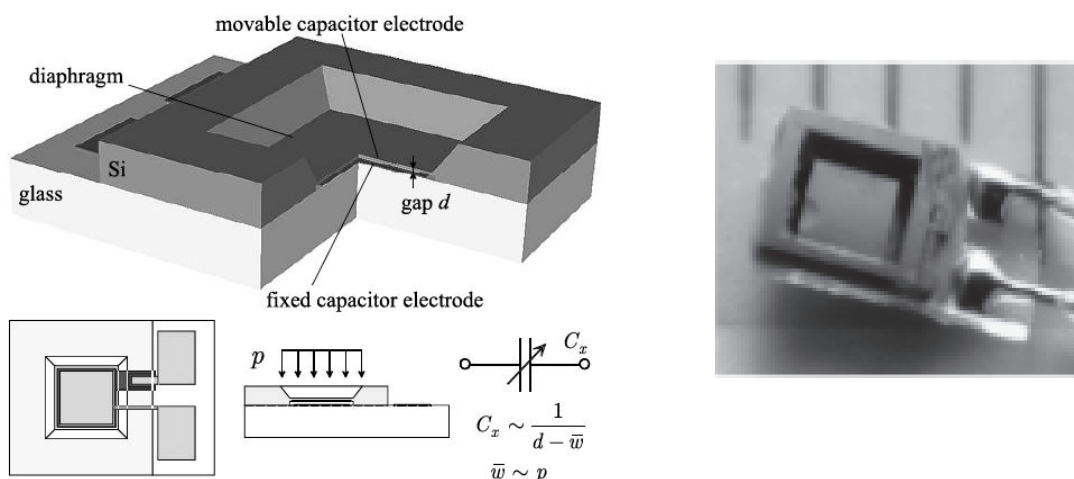

Figure 1 : Schematic representation of the capacitive pressure sensor and device picture

Firstly, the reference cavity that determines the capacitor plate separation is etched on the epi side of the wafer. A typical cavity depth or zero-pressure plate separation is 1 µm. Hence, the zero pressure capacitance C_0 lies in the order of 10 pF. The thickness of the diaphragm can be accurately controlled e.g. by the application of a 2-electrode p-n junction etch stop technique in a (KOH/$H_2$0) solution [2, [3]. A sputter-deposited Al layer (typically 100 nm) on a borosilicate glass wafer serves as the top (fixed)

capacitor plate. Figure 2 represents a measured pressure characteristic of the described micro-sensor. Note the very high pressure sensitivity : the capacitance change induced by the full scale pressure is higher than 100 % of the zero pressure capacitance. This capacitance swing is impressive compared with the 3 % swing (or less) for a piezo-resistive device.
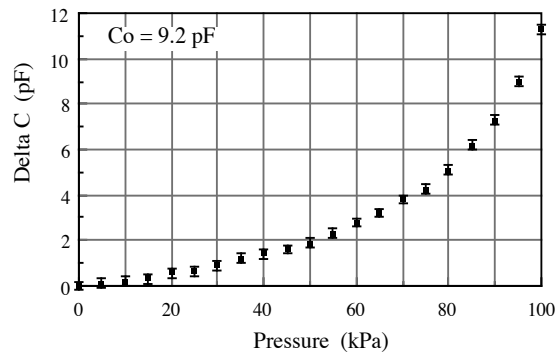

Figure 2: Measured characteristic of capacitance versus pressure, with impressive sensitivity

Excellent temperature behaviour is known to be another specific merit of the capacitive transducer principle [4, 5]. However, this is only true if the sensor is sealed in vacuum, which yields an absolute pressure sensoror for a full differntial sensor. The measured output impedance is capacitive and is typically as large as 300 MΩ at 50 Hz. Therefore, the capacitive sensors are very susceptible to environmental noise and their application is restricted to very well shielded environments, unless an impedance conversion is performed inside the sensor package itself. The presence of parasitic or stray capacitances C_p causes the total capacitance to be only partially sensitive to pressure. These parasitic capacitances become relatively more important for smaller values of the sensing capacitance C_x, i.e. for smaller applied pressures. Hence, the sensor characteristics will be distorted in the lower part of the pressure range.

As pointed out in the previous paragraph, the objective of an interface circuit for miniature capacitive pressure sensors are threefold. First, a conversion to a low impedance output is imperative. Second, a first order linearization can be achieved by inversion of the capacitance versus pressure relationship, in combination with sensors of the stiffened membrane type. Third, parasitic capacitances, leakage resistors and electrostatic induced 'pressures' must be suppressed. To achieve this, a typical conversion circuit will look like figure 3 [2]. It compensates for the main intrinsic deficiencies of the capacitive transducers. The small absolute capacitance changes are converted into a voltage output at low impedance. A first-order linearization is obtained by inversion of the hyperbolic C-P relationship. Moreover, a second-order linearization is achieved by an active suppression scheme for parasitic capacitances to the substrate. This reduces parasitics to an apparent value in the order of 0.1 pF, even if they initially were an order of magnitude larger than the sensing capacitance.
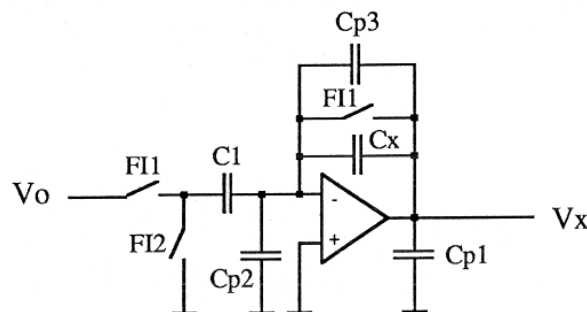
Figure 3 : Basic conversion circuit, to yield first order linearisation, and rejection of parasitics

The origins of the parasitic elements in such capacitive sensors is illustrusted in figure 4. These consist in Cp1, the capacitor between the movable electrode and the substrate, in the case shown the inversly biased junctions, Cp2, the capacitor of the fixed plate to the substrate, and Gp, the parallel impedance, comprising both a leakage resistor and another parasitic capacitor (between the connecting wires)

Figure 4 : Origins of parasitics : sense capacitor *Cx*, parasitic shunt conductance *Gp* and parasitic capacitances *C*p1 and *C*p2. Cp1 is illustrated to the left.

The suppression performance of the proposed circuit is impressive : a PCRR (parasitic capacitance rejection ratlo) can be defined as the ratlo of the suppressed C, over the unsuppressed C, causing the same nonlihearity The PCRR for Cp1 is -80 dB in the given example The PCRR for Cp2 is -50 dB

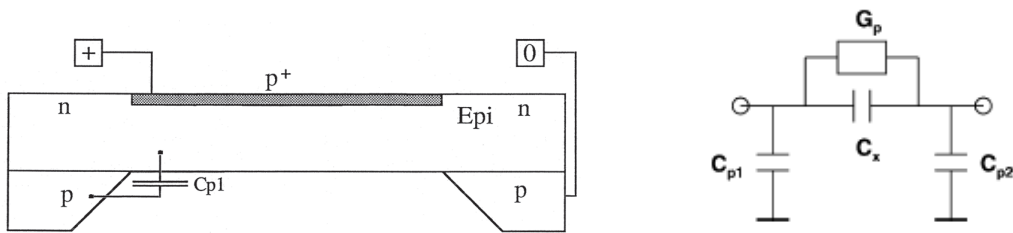On the other hand the introduction of an interface circuit must not impair any of the specific advantages of the transducer principle. Therefore low power consumption, low temperature sensitivity and high resolution and stability are the most important requirements. Switched capacitor techniques have been applied to meet the specifications of power consumption and resolution. The supply current can be as low as 30 μA for a 3 V supply, resulting in a pressure sensing resolution of 4 to 5 decades and sensitivities up to 1.75 mV/V mbar for a 500 mbar range. A differential measuring set-up can be chosen to cancel effects of temperature sensitivity and to increase stability. The complete interface circuit consists of digital circuitry (clock generator, flip-flops, divider, logic gates) combined with analog circuitry (opamp's, voltage reference, current reference, comparators) on the same CMOS-chip (figure 5). Figure 5 also shows the measured output voltage characteristic of a relative capacitive pressure sensor and the same sensor coupled to the dedicated processing circuit [2].

$$Vout = Vo.C1.(\frac{1}{Cref} - \frac{1}{Cx})$$
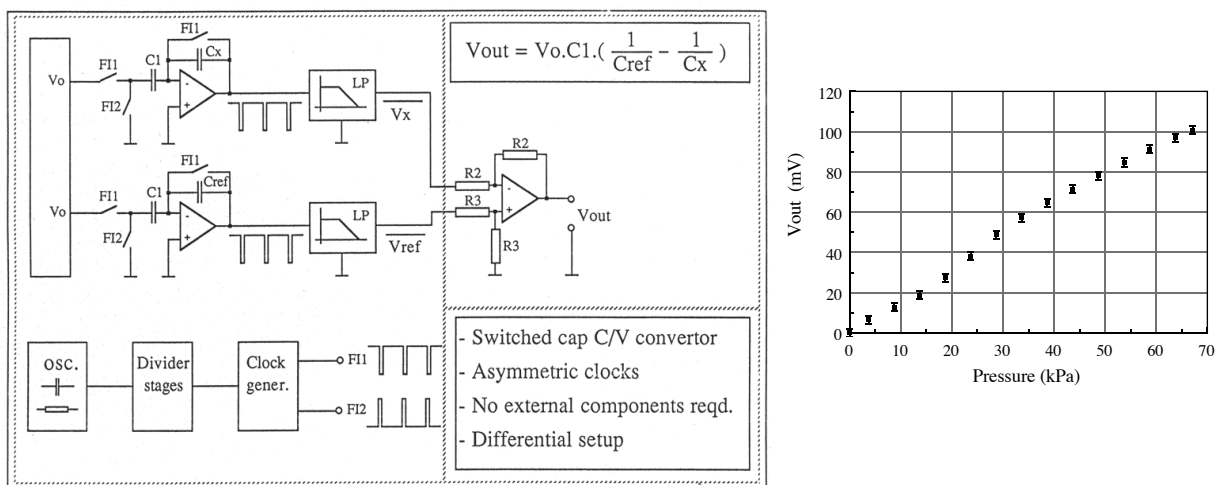
Figure 5 : Complete differential circuit. (C_{ref} can also be the antiphase capacitor in e.g. accelerometers) Measured output characteristic for a capacitive pressure sensor with interface

General purpose interface with reduction of opamp offset effects

The drive towards an intelligent environment has lead to an increased need for intelligent and independent sensors. The emerging possibilities of these autonomous sensors will give impulse to several new applications like intelligent prostheses [6, 7], sport evaluation [8], measurement and prediction of weather patterns [9], etc. Conventional sensor interfaces are specifically tailored towards the requirements of one of these applications. This leads to a high design cost for every new autonomous sensor system. An ultra low power generic sensor interface offers an attractive solution for this problem. It allows us to adapt the front-end after it is taken in use. Moreover, a generic interface is capable of reading out several sensors in different time intervals.

Ultra low power (ULP) consumption (<100 μW) is an important issue in the design of such a system. This results in a long lifetime for battery operated systems and enables fully autonomous sensor systems powered by energy scavengers. In addition, the generic interface should not come with a significant energy penalty. The new design methods reported in this paper allow us to create a generic sensor

interface with a minimum loss. Furthermore, an algorithm is provided, which calculates the optimal interface settings for each application.

The general purpose interface circuit contains a microcontroller interface, a configuration memory and the following configurable blocks (Fig. 6): an LF clock, a sample timer, a bandgap reference and bias circuits, a main oscillator and clock generation circuits, capacitance-to-voltage (C-V) converters, an SC amplifier, a voltage-to-current (V-I) converter, a modulator, a decimation counter and a conversion timer.

Figure 6 : Functional description of a general purpose interface circuit concept

The proposed readout circuit provides an interface to single and differential capacitive sensor applications with 1 pF $<Co<$ 15 pF and 200 fF $<\Delta C<$ 10 pF; parasitics range : $Cp1$ <50 pF and $Cp2$ <50 pF.

The SC interface converts a capacitance variation to a proportional voltage. It consists of two C-V converters and an SC amplifier. In the C-V converters, the sense capacitance is converted to a proportional voltage. The SC amplifier amplifies the difference between the outputs of the C-V converters and produces a quasi-continuous input voltage for the $\sum\Delta$ modulator (V-I converter and modulator). The main oscillator and clock generation circuits provide the clock signals to the capacitive sensor interface and the decimation counter. The reference and bias circuits generate the bias currents for the SC interface, the $\sum\Delta$ modulator and the main oscillator. The SC interface, the $\sum\Delta$ modulator, the main oscillator, the reference and the bias circuits are only powered in active mode ('Act' is high). The LF clock and sample timer are used for the timing during low-power standby operation. Therefore, they are implemented with a very low current consumption of approximately 500 nA.

Many capacitive sensor interfaces use the sensor directly in a $\sum\Delta$ modulator structure [10, 11]. This leads to high power consumption, because the capacitors must be charged and discharged on the rhythm of the high oversampling clock of the modulator. Most of these sensor interfaces are designed for closed loop accelerometers. In these circuits, the electrostatic feedback force is used to keep the sensor mass in its balanced position, which results in a high linearity. Hence, the mechanical transfer characteristic acts as a second order filter in the feedback loop. As a consequence, the stability and the performance of the readout circuit strongly depend on the specific sensor [12]. Moreover, these systems need an important start-up time to bring the sensor mass close to equilibrium [13]. Hence, it is not possible to operate them in a power efficient duty cycle.

Figure 7 shows the front-end architecture that consists of a switched capacitor (SC) interface followed by a $\sum\Delta$ modulator. The SC interface works on a lower clock frequency, 8 kHz, than the modulator, 128 kHz, to reduce power consumption [14]. In the capacitance-to-voltage (C–V) converter, the sense capacitance, Cx, is converted to a proportional voltage. The SC amplifier amplifies the difference between the outputs of both C–V converters and produces a quasi continuous input voltage for the sigma delta modulator. The capacitive sensor interface has two modes of operation.

The first mode is for single sensor operation with on chip reference capacitor, where the reference capacitor $Cref$ needs to be programmed to approximate $C0$. The other mode is for differential sensor (or

single sensor with off chip reference) operation, where the on chip reference capacitor is not used. In both modes, the amplification factor *ASC* of the SC amplifier and the feedback capacitor *Cf* of the *C–V* converters need to be programmed for optimal accuracy of the interface.
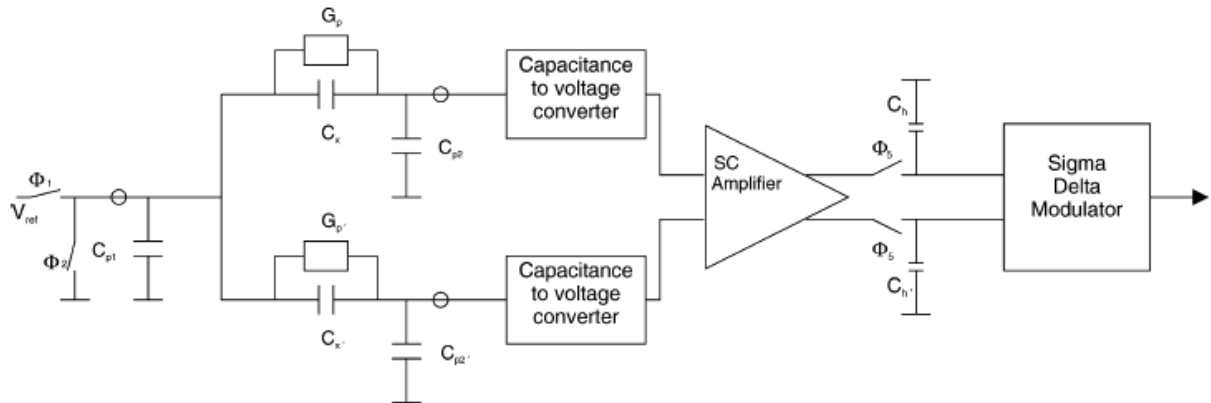

Fig. 7. Capacitive sensor readout architecture with a differential sensor.

Fig. 8 shows the C-V converters and the SC amplifier. At the end of the signal phase, assuming an ideal charge transfer, the voltage at the output of the C-V converter equals Vref.Cx/Cf. In reality, the charge transfer will be imperfect due to the finite transient response of the operational trasconductance amplifier (OTA). This transfer error has two contributions: the leakage error and the settling error. The potential will settle in a certain time to the virtual ground, during this time some charge will leak away through the parasitic shunt conductance, Gp, resulting in a leakage error. At the end of , the potential will be slightly different from the ground level, so a small charge remains on Cp2+Cx, resulting in the settling error. The Correlated double sampling (CDS) operation reduces the effects of offset and 1/f noise of the OTA. The proposed chopping scheme provides a solution for this problem. In this scheme, a pseudo differential structure is built, where the capacitive sensor elements are connected to each C-V converter for an equal number of interface periods. This modulates the effects of the mismatch withthe chopping sequence. These components are filtered by thelow-pass operation of the ∑Δ modulator.
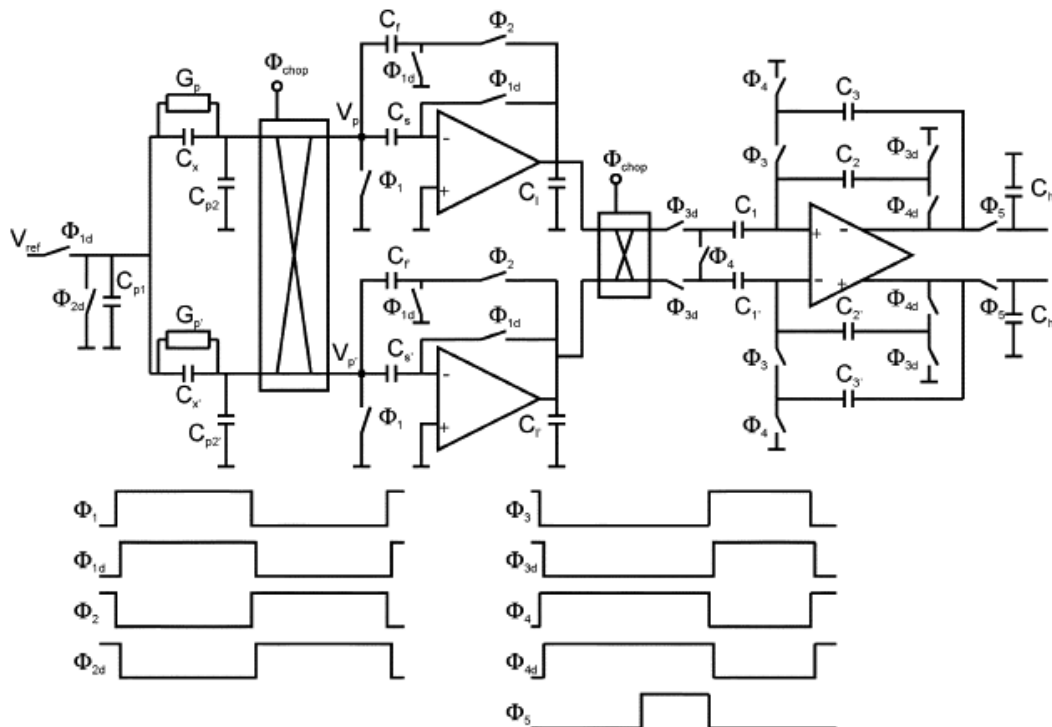

Figure 8 : SC interface with two C–V converters, SC amplifier, chopping scheme, and clocks.

Conclusions

The increasing performance of smart microsystems merging sensors, signal processing and wireless communication promises to have a pervasive impact during the coming decade. A generic front-end architecture, where only the sensors and the microcontroller software are customized to the selected application, would reduce the costs significantly. Previous generic readout circuits were mainly designed for industrial applications. Hence, they do not meet the stringent power requirements (tens of microwatts), which are necessary for long term autonomous sensing.

It is shown how sensor interfaces should be conceived for these sensors, and examples are given to both reduce the susceptibility to parasitic capacitances, as well as how to reduce offset problems. Moreover, by adding programmability, it is possible to provide a generic interface in the same package.

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