

A 64 x 48 BSI SPAD Sensor Based on 8" Wafer 3D Stacking Technology

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Summary: A 3D stacking process by direct wafer bonding and the resulting sensor are presented to emphasize the potential of this technology for future sensor developments. By using the Fraunhofer IMS own 0.35 μm CMOS and micro systems technology, a 64 x 48 pixel sensor containing backside-illuminated low-noise single-photon avalanche diodes and in-pixel time-to-digital converters was fabricated. It is being applied on light detection and ranging applications as well as quantum imaging and characterized in both photon timing and counting mode.

Keywords: BSI SPAD, wafer bonding, 3D integration, 3D stacking, single-photon detection, LiDAR, ToF, quantum imaging

Background and Motivation

Single-photon detection with high temporal resolution is crucial for many rising application and research fields like light detection and ranging (LiDAR), quantum imaging, quantum random number generation (QRNG), fluorescence lifetime imaging (FLIM), spectroscopy and more. Single-photon avalanche diodes (SPADs) provide the preferred solution due to high performance in terms of detection efficiency, noise and timing jitter as well as the possibility of integration into complementary metal-oxide-semiconductor (CMOS) technology. On-chip circuits to obtain timing information are complex and introduce a high space consumption which eventually limits the fill factor and sensor sensitivity. Smaller CMOS technology nodes offer improvement but come with a higher dark count rate (DCR) which ultimately increases the sensor noise level [1]. 3D integration techniques allow vertical arrangement of readout electronics and SPADs to increase the fill factor and enable backside-illumination (BSI). While chip-to-wafer bonding offers a viable solution, direct wafer bonding with post-processing is the preferred option for higher volumes. Another crucial benefit is introduced by the possibility to combine different technology nodes and thus exploit both small-scale electronics and high performance SPADs.

Architecture

The presented sensor has an area of 10.25 mm by 9.2 mm while the active area claims 8.3 mm by 6.2 mm. The array consists of 64 x 48 pixels with 4 SPADs in each pixel which are connected by an adaptive coincidence circuitry which

enables background light rejection [2]. Time-to-digital converter (TDC) sharing of 4 pixels with two storable timestamps per measurement cycle allows for a pixel pitch of 130 μm . The sensor is capable of photon counting (9 bit) and timing with 312.5 ps bin width during a 1.28 μs full scale range.

Direct wafer bonding

The readout integrated circuit (ROIC) and SPAD 8" wafers are fabricated separately in 0.35 μm automotive certified P1M4 and custom sensor technology, respectively. Surface roughness is a crucial parameter for the bond reliability and quality with a widely accepted threshold for successful hydrophilic bonding of a root mean square (RMS) roughness of below 0.5 nm [3]. This was achieved by a multi-stage chemical mechanical planarization process with several oxide depositions. Additionally, both wafer layouts are optimized to enhance homogeneity and avoid sites for possible topography variances. Typical values of the surface roughness before the bonding process were determined to be 0.25 – 0.3 nm RMS.

Hydrophilic low-temperature direct wafer bonding is used to establish a stable connection. Therefore, the wafer pairs are being aligned and put into contact with an alignment precision below 1 μm . Finally, the wafer pair is annealed at a temperature of 350°C.

Post-processing

To give access to the SPAD active areas that are close to the interface after bonding, the top wafer is thinned down to approximately 5 μm thickness. This is done by silicon etching with

an etch stop on the buried oxide layer of the silicon-on-insulator (SOI) wafer. The electrical contact between the wafers is established by front side through-silicon-vias (TSV). Here, bi-level silicon oxide etching exposes the ROIC and SPAD wiring metal which are then connected by sidewall deposition of an optimized material stack via physical vapour deposition (PVD) and atomic layer deposition (ALD). The bond pads are exposed in a subsequent etching step for accessibility during packaging. The schematic cross section of a wafer stack after post-processing can be seen in Fig. 1.

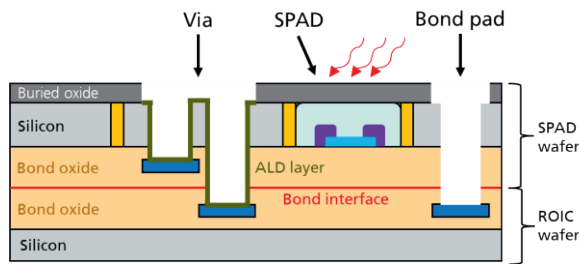


Fig. 1. Schematic cross-section of the final wafer stack configuration

Results

Scanning acoustic microscopy (SAM) was used to prove the bond result with the ability to reveal voids in the interface. An exemplary SAM image is shown in Fig. 2. It shows that a stable bond connection was established with few voids covering only dies near the wafer edge which were not fully exposed.

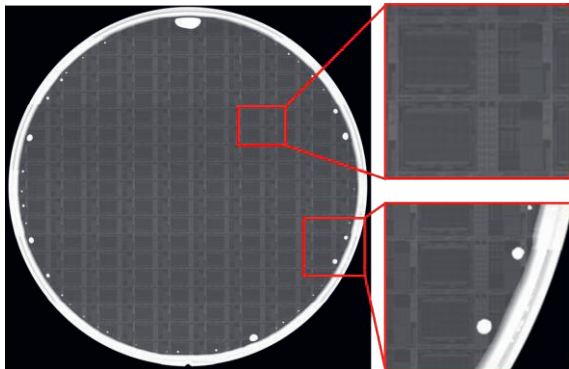


Fig. 2. SAM images of an 8" wafer bond with few voids near the wafer edge

The TSV design and processing forms a reliable electrical interconnection between the wafers with an average resistance of 14 Ω /TSV. This value was determined by testing a series connection of up to 170 TSVs in daisy chain structures. The TSV reliability was examined according to AECQ100 grade 1 and JESD2A104E, including 500 temperature cycles from -65 to 150 $^{\circ}$ C. No failures and a neglectable resistance change of < 5% were observed.

The BSI SPADs show a very low median DCR of 0.9 cps/ μm^2 , which is one of the lowest recorded and can compete with frontside illuminated SPADs, which typically show lower values [4]. The overall performance of the BSI SPAD sensor was evaluated in both photon timing and photon counting mode, as exemplarily shown in 3D (time-of-flight) and 2D images of a street view with a row of garages in Fig. 3.

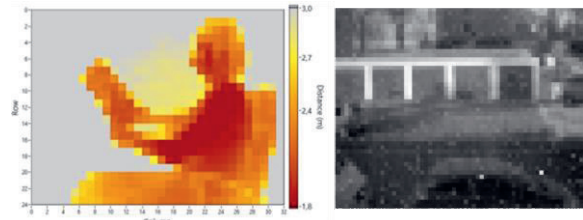


Fig. 3. Sensor operation in photon timing (left) and counting mode (right)

For time-of-flight imaging, this sensor provides a maximum range of 192 m with a depth resolution of 4.7 cm. The coincidence circuit reduces the probability for the detection of background generated events and thus improves the ability to separate between ambient light and laser signal while being able to adapt to the background event rate.

Conclusion

A reliable process for wafer bonding and post-processing for 8" CMOS wafers was developed and demonstrated with the fabrication of a 64 x 48 BSI SPAD sensor. A stable bond interface, reliable via structures and low DCR SPADs are presented. The sensor functionality and performance can be shown in photon timing and counting mode. The developed 8" wafer 3D stacking process enables the combination of technology nodes aiming at both small-scale electronics and low DCR BSI SPADs with the possibility of low to high volume production in future sensor developments.

References

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