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Electrochemical Seismometers Using a SOI Chip with Four Micro-electrodes

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Summary:

This paper reports a new method to integrate four micro-electrodes on one SOI wafer with micro-vias of any size. 6 different SOI chips with nice insulation between each electrode was fabricated. After the test of electrochemical seismometers (ECSs), it shows that the ECSs using the chips with large diameter and small minimum inter-space of micro-vias feature small bandwidth but large peak sensitivity, which provides a valuable reference for the design of the ECSs meeting different performance.

Keywords: SOI, micro-electrodes, micro-vias, MEMS technologies, electrochemical seismometers.

Background, Motivation an Objective

Four micro-electrodes arraying on the sequence of anode-cathode-cathode-anode is the sensitive element of electrochemical seismometers (ECSs). They are typically formed on chips with numbers of micro-vias [1-3]. With the growingly development of the MEMS technologies, the tendency of them is to reduce the consumption of wafers and to increase the integration of electrode areas. In recent years, the number of electrodes fabricated on one wafer had already increase from one[1], two[2] to lately four[3]. However, the method presented by reference [3] was only applicable to chips with the micro-vias with large depth-to-diameter ratios. This paper supposed a new fabrication process of a SOI chip with four micro-electrodes, which could make vias of any size. 6 SOI chips were fabricated to compare the influence of different structural parameters on the performance.

Description of the New Method or System

This paper proposed a method to fabricate SOI chips with four micro-electrodes on one wafer. On the beginning, a SOI composed of two 200μm thick silicon and one 2um thick SiO_2 was prepared. After twice lithography and Deep Reactive Ion Etching (DRIE), the removal of the SiO_2 was achieved by using hydrogen fluoride to form insulating slot. Insulating layers of SiO_2 were firstly deposited on the both surfaces of the wafer by Chemical Vapor Deposition (CVD) before sputtering platinum on that. Finally, excess metal was removed by Ion Beam Etching (IBE), where the retained metal was protected by dry film.

Results

Six different SOI chips with four micro-electrodes having nice insulation between each electrode were fabricated. By assembled in a same ECS and using a same testing circuit, their response of sensitivity vs frequency was tested as the figure showed. The results supposed that the chips with large diameter and small minimum inter-space of micro-vias achieved small bandwidth but large peak sensitivity, of which the ECS using chip-1 had the smallest bandwidth of 2.90Hz-7.60Hz and the largest peak sensitivity of 12962.03V/(m/s)@5Hz. To the contrary, the ECS using chip-6 had the largest bandwidth of 0.84Hz-34.21Hz and the smallest peak sensitivity of 4098.83V/(m/s)@3Hz. This provided a valuable reference for the design of the ECS meeting different performance requirements.

References

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Figures

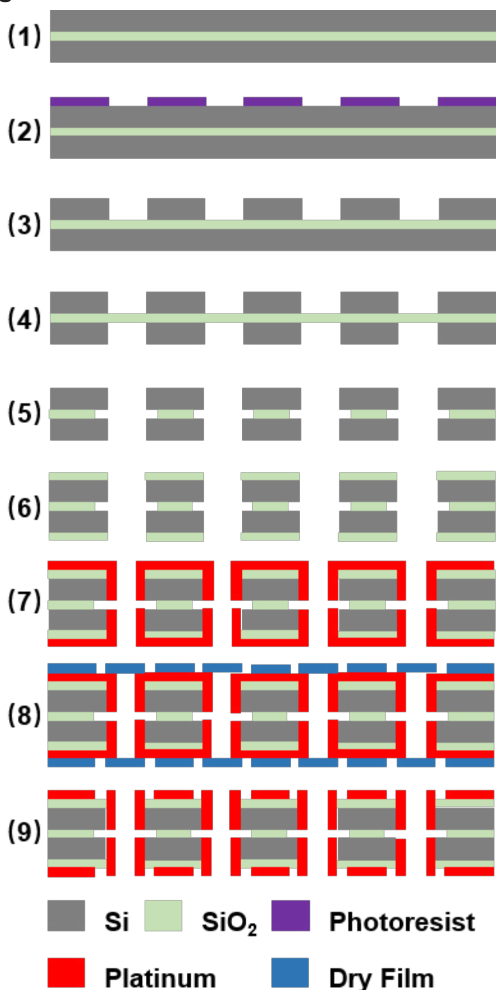

Fig. 1. Fabrication Process of a SOI chip with four micro-electrodes.

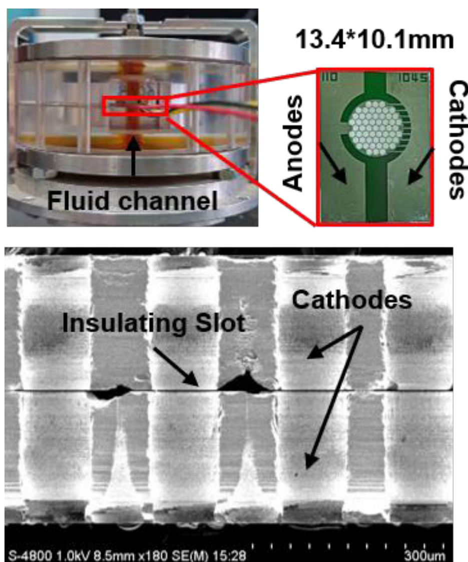

Fig. 2. Physical diagram of a MEMS electrochemical seismometer and a SOI chip with SEM diagram of its cross section.

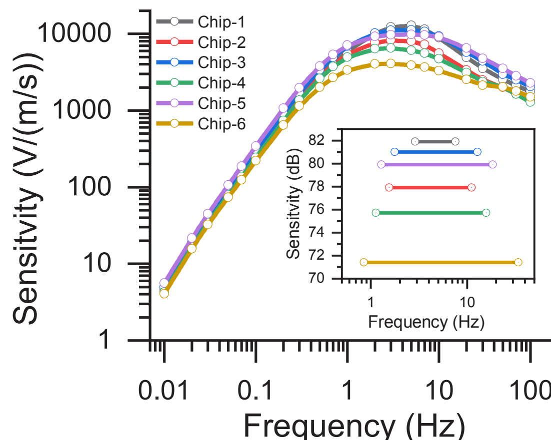

Fig. 3. Graph of sensitivity vs frequency for six different SOI chips, where the mini-graph is the bandwidth of them.

Tables

Tab. 1: Structural parameters of six different SOI chips

	Diameter of micro-vias	Minimum inter-space of micro-vias
Chip-1	110µm	10µm
Chip-2	100µm	15µm
Chip-3	90µm	10µm
Chip-4	80µm	15µm
Chip-5	70µm	10µm
Chip-6	60µm	15µm

Tab. 2: Bandwidth and peak sensitivity of six different SOI chips

	Bandwidth	Peak sensitivity
Chip-1	2.90Hz-7.60Hz	12962.03 V/(m/s)@5Hz
Chip-2	1.55Hz-11.15Hz	8262.24 V/(m/s)@3Hz
Chip-3	1.77Hz-12.87Hz	11318.51 V/(m/s)@5Hz
Chip-4	1.13Hz-15.80Hz	6524.09 V/(m/s)@3Hz
Chip-5	1.29Hz-18.55Hz	9851.62 V/(m/s)@5Hz
Chip-6	0.84Hz-34.21Hz	4098.83 V/(m/s)@3Hz