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Accurate silicon epitaxial multilayer characterization for CMOS imager applications

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Summary:

Silicon epitaxial layer technology provides a key building block for charged particle tracking devices, eg. complementary metal-oxide semiconductor (CMOS) active pixel sensors. Such detector elements are realized on a thick (~775um) heavily doped top quality 12” silicon substrate with a subsequent thin (~1-20um) lightly doped silicon epitaxial layer or multilayer deposition. This epitaxial layer structure also provides virtual substrate for further CMOS manufacturing steps, relatively free of metal contamination and/or crystallographic defects [1,2].

Accurate characterization of such structures, in terms of multilayer thickness, dopant concentrations, and buried defect density is possible with advanced optical instrumentation [3-6]. A round-robin test series were conducted on typical samples with silicon epilayer structures, including Fourier-transform infrared (FTIR) reflectometry, with results confirmed by spreading resistance profiling (SRP) and imaging photoluminescence (PL) techniques.

Keywords: silicon, epitaxial layers, epi, FTIR, spreading resistance profiling, CMOS, imaging sensors

Results:

Advanced optical modeling was applied to the acquired infrared reflection spectra on Si wafers with epitaxial multilayers. A typical result is shown in Fig. 1, where the so-called transition zone (TZ) in between the epilayer and the substrate was modeled by a series of sub-layers with varying charge carrier density.

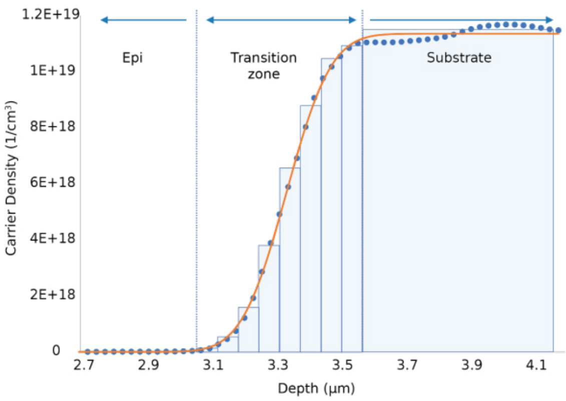

Fig. 1. Characteristic result of the applied advanced infrared optical modeling on Si epilayer structures.

The obtained optical carrier density profile was confirmed by a direct electrical technique, spreading resistance profiling (SRP). Fig. 2 shows the edge of the samples that were beveled at a shallow angle to prepare them for SRP measurements.

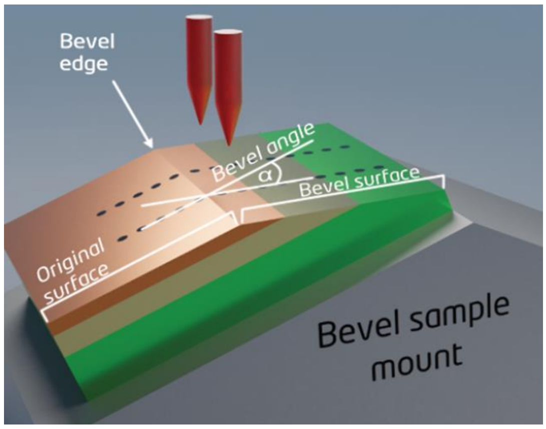

Fig. 2. Schematic diagram of the SRP measurement sequence

Common methods for detecting defects related to epitaxial layer gworth in silicon are usually time-consuming and often destructive. By contrast, Semilab’s PL imaging technique (so-called EnVision) provides a quick, non-destructive way of finding these defects [4-6]. Additionally, the online neural network-based analysis offers classification of the found defects. The obtained results are consistent with traditional etch-based methods [4]. Validation of the PL results were performed by semiconductor reference fabs on processed electronic devices, as shown in Fig. 3.

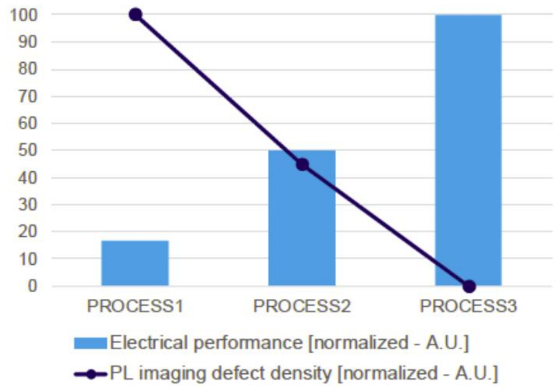

Fig. 3. Reduction of defect cound achieved during optimization of process used for P-N junctions in CMOS imager devices [5]

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