DOI 10.5162/SMSI2025/C2.1

„Sensor-Intelligence Devices (SID) for optimized condition and process monitoring“

K. Becker[1], D. Koster[1], H.-G. Herrmann[1];
[1]Fraunhofer-Institut für Zerstörungsfreie Prüfverfahren IZFP; Campus E3 1; 66123 Saarbrücken, Deutschland
kevin.becker@izfp.fraunhofer.de, Dirk.Koster@izfp.fraunhofer.de, Hans-Georg.Herrmann@izfp.fraunhofer.de

Summary:
In-memory computing (IMC) has gained significant attention in recent years, particularly in the context of energy-efficient sensor systems and the emerging field of ultra-low power and Tiny Machine Learning (TinyML).[3-4] In this work the capability of an SRAM memory to process Machine Learning algorithms for Sensor-Intelligence Devices (SID) could be demonstrated.

Keywords: SRAM, Machine learning processing, compute in memory, mixed-signal computing, analog in-memory computing

Background, Motivation and Objective

Intelligent sensor-systems are revolutionizing data processing by integrating AI directly into sensor systems, enabling real-time analysis and decision-making at the edge. Unlike traditional sensors, SIDs fuse multi-modal data, leverage neuromorphic computing, and utilize in-memory processing to maximize efficiency [1]. Techniques like compressed sensing and TinyML are enhancing this capability in reducing power-consumption and maintaining a high performance. Energy-efficient AI processors play a crucial role in advancing SIDs, particularly for edge computing. Innovations such as low-power NPUs, quantization, and sleep-mode optimization are enabling AI inference on battery-powered devices. Also extending operational lifetimes in remote and power-constrained environments. Near-sensor-computing is transforming industries such as material testing, manufacturing, healthcare, defense, and civilian security. In industrial applications, they enable predictive maintenance and automated defect detection, reducing downtime and improving quality control. In healthcare, wearable SIDs can provide real-time diagnostics. Deploying intelligent sensor-systems in remote and inaccessible locations presents challenges, including energy constraints, intermittent connectivity, and harsh environmental conditions. Advances in low-power design,

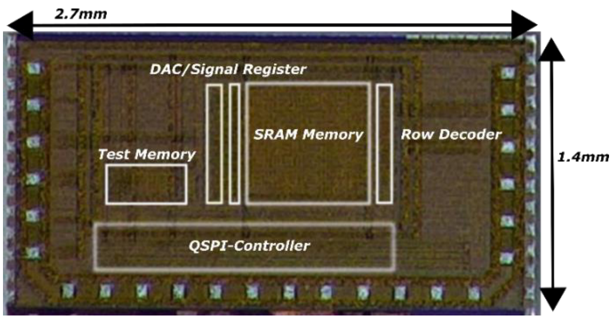

Figure 1 Picture of the chip. It includes the SRAM memory with its peripheral components

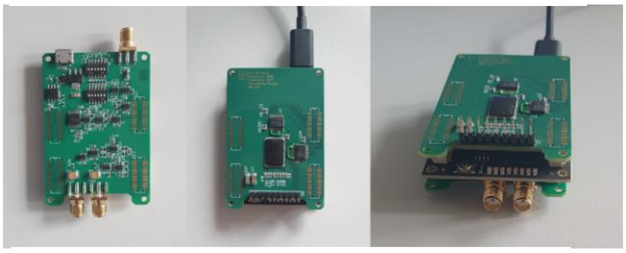

Figure 2 Eddy current transceiver, ASIC-PCB and completely stacked sensor-system

DOI 10.5162/SMSI2025/C2.1

LPWAN communication, and self-diagnostic capabilities ensure long-term autonomous operation. By processing data locally, SIDs reduce cloud dependency, enhance privacy, and enable AI to function reliably in real-world, power-sensitive applications. These innovations pave the way for a new era of pervasive, low-energy AI, making intelligent systems more accessible and sustainable across diverse industries [2].

Description of the New Method or System

This work introduces a novel 6T-SRAM-based In-Memory Computing (IMC) method implemented in a 180nm technology node shown in *Fig.1*. The key innovation lies in the analog computation within the memory of the SRAM by integrating 128 polysilicon Digital-to-Analog Converters (DACs) near the memory. This enables data processing, in terms of efficient multiply an accumulate operations, with a minimal footprint, low power consumption, and high energy efficiency shown in Fig.4. The DAC generate an analog voltage, that modulates the conductance of pass transistors, effectively performing element-wise multiplication. The charge from all bitcells of the memory is then accumulated across the bitline. The voltage measured by the comparators at the bitlines is then used as activation function. The proposed method is designed for real-time sensor data classification, specifically targeting eddy current sensor systems. The classification process is executed directly within the SRAM, leveraging an in-memory algorithm that processes sensor data collected from an eddy-current transceiver *Fig.2*. The system incorporates an FPGA for signal preprocessing and sensor excitation, utilizing a transceiver to measure impedance variations across different materials. This approach offers significant advantages in performance density and energy efficiency. This new IMC approach paves the way for energy-efficient, high-performance machine-learning applications in embedded sensor systems.

Results

The SRAM-based In-Memory Computing (IMC) accelerator successfully classified real-world sensor data for nondestructive testing (NDT) using eddy currents. The fabricated chip achieves 3.2 TOPS/mm², while simulations of the 16kb IMC core predict 45 TOPS/W at 50 MHz. Experimental validation at 5 MHz confirms an energy efficiency of 3.4 TOPS/W. The system, including a sensor setup and computer interface for data storage, was tested with an external 5 MHz clock controlling the digital processing. The classification task demonstrated 98% accuracy in distinguishing different materials using multiple datasets across various bitlines. The measured power consumption of the chip averaged 48 mW, with an energy efficiency of 3.4 TOPS/W. Training all bitlines using an external PC took 1700 seconds per bitline over 20 iterations. For inference, the primary source of power consumption was identified as the DACs, leading to an optimized design that reduces DAC power consumption by a factor of 25, targeting a maximum current of 1 mA. This new version is currently under fabrication. The DAC power consumption varies based on the input signal due to the current drawn by the R2R ladder DACs, which depends on the digital input code. While larger DACs can reduce power consumption, they increase the overall chip size. However, using polysilicon resistors ensures high output linearity, making this design an effective trade-off. A key advantage of this approach is that standard memory components are repurposed for computation, enabling direct processing within memory rather than limiting the system to conventional read/write operations.

Table I

CHIP SPECIFICATIONS

	Measurements and Specification
Process	180nm
Computation Type	IMAC
Architecture	Mixed-Signal
Cell Structure	6T
I/W/Out	8/1/1
Performance	3.2TOPS/mm^2
Efficiency	3.4TOPS/W
Circuit Area Overhead	6%
Core Size	670µmx900µm

Figure 3 Overview of the chip specification and measurements

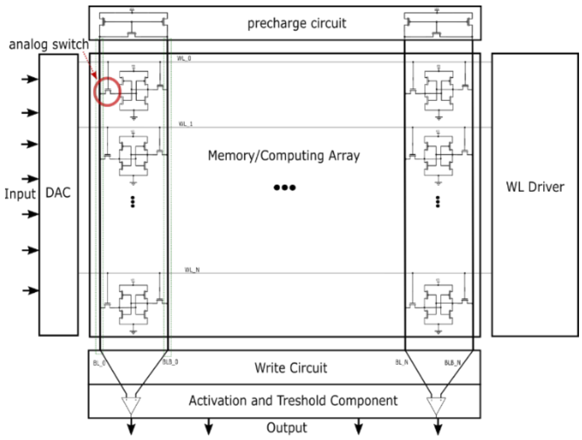

Figure 4 In-Memory Computing Technique within SRAM Memory

Conclusion

This work presents a high-performance IMC architecture that can be used for real-life datasets for eddy current testing while reaching an energy efficiency of 3.4 TOPS/W with a small area overhead, in concern of the integrated 128 DACs, of about 6% of the total chip area successfully implemented in different industrial projects, such as for the investigation of load and the motion of wall anchors via accurate position- and distance measurements. Results in research projects for the determination of the humidity of concrete at bridges leading to structural damages like corrosion at the reinforcement or spalling due to volume increase are not yet available but look very promising.

Acknowledgement

This work was supported by the Saarland Ministry of Economic Affairs, Innovation, Digital and Energy (MWIDE) and the Fraunhofer Ge-sellschaft (High-Performance Center ‘Sensor-Intelligence’).

References

[1] S. Paul, R. Karam, S. Bhunia and R. Puri, "Energy-efficient hardware acceleration through computing in the memory," 2014 Design, Automation & Test in Europe Conference & Exhibition (DATE), Dresden, Germany, 2014, pp. 1-6, doi: 10.7873/DATE.2014.279

[2] H. Ahlendorf and L. Göpfert, "Hardware/software design challenges of low-power sensor nodes for condition monitoring," 2010 Design, Automation & Test in Europe Conference & Exhibition (DATE 2010), Dresden, Germany, 2010, pp. 659-659, doi: 10.1109/DATE.2010.5457122.

[3] S. K. Gonugondla, C. Sakr, H. Dbouk and N. R. Shanbhag, "Fundamental Limits on the Precision of In-memory Architectures," 2020 IEEE/ACM International Conference On Computer Aided Design (ICCAD), San Diego, CA, USA, 2020, pp. 1-9.

[4] N. Verma et al., "In-Memory Computing: Advances and Prospects," in IEEE Solid-State Circuits Magazine, vol. 11, no. 3, pp. 43-55, Summer 2019, doi: 10.1109/MSSC.2019.2922889