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Simultaneous Analysis of Local Device Layer Thickness and Film Stress on Cantilevered MEMS Structures

Dominik Huber[1], Christoph Schallert[1], Georg Pfusterschmied[1], Ulrich Schmid[1]
[1] TU Wien, Institute of Sensor and Actuator Systems, Gußhausstraße 27-29, 1040, Vienna, Austria
Dominik.Huber@tuwien.ac.at

Summary:

This paper reports on a passive MEMS structure facilitating the local measurement of both, the device layer thickness and residual film stress with white light interferometry (WLI). The structure consists of a released single-side clamped plate (SSCP) and a step-profile etched through the device layer down to a silicon dioxide layer. In doing so, both the static deflection and the thickness are determined, independent of material parameters, such as the index of refraction or surface roughness. Both key properties can be efficiently measured with the same tailored WLI set-up.

Keywords: device layer thickness, film stress, WLI, SiC, automation

Background, Motivation, and Objective

Tolerances of the device layer properties, such as thickness or residual stress are common for standard SOI wafers in the MEMS industry as well as for any thin films deposited during device fabrication[1, 2]. Ellipsometry is a well-established technique for the analysis of the thickness of thin films [3]. It is a fast and non-destructive technique to measure the impact of the thin film on polarized light. To calculate the thickness of a thin film from that measurement, precise knowledge about material parameters, e.g., index of refraction, is necessary, and a smooth surface is highly recommended. On wafer-level the curvature measurement is widely applied to calculate the residual stress from Stoney's formula [4]. This technique has the disadvantage, that it is developed for uniform thin film thickness, which led to extensive progress on passive test structures for optical measurements of the static deflection[5, 6]. However, there is still the need to determine both parameters, static deflection, and thickness, with the same WLI set-up on-chip with a fully automated approach.

Description of the New Method or System

In this study, we present the simultaneous measurement of the static deflection of released SSCP structures and the device layer thickness with the same WLI set-up. This combination allows for the development of a high-precision residual stress map across a wafer with minimal time consumption. Test structures consisting of an SSCP and a step-profile close to the anchor region are presented in *Figure 1*. The step-profile consists of 50 µm wide trenches etched through the device layer. Utilizing deep reactive ion etching (DRIE), the plates are released from the substrate, whereas the stress in the device layer leads to a static deflection. Plates with a constant length of 500 µm and different widths ranging from 50 µm to 1000 µm were fabricated, enabling the characterization of local stress profiles. In general, a straightforward integration of such test structures is possible for MEMS devices, achieving local information, such as thin film thickness and in further consequence, the intrinsic film stress.

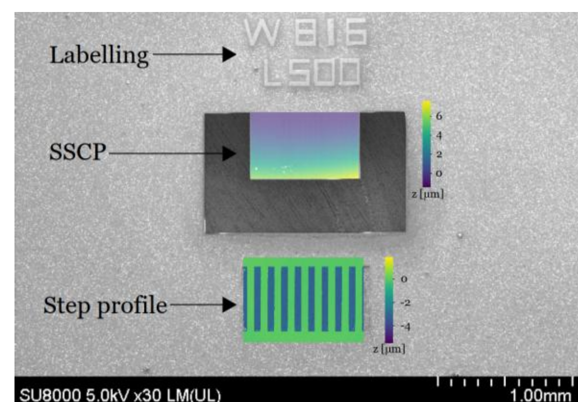

Figure 1: SEM image of the MEMS structure consisting of an 816 µm wide and 500 µm long SSCP released from the back, and a step-profile with 10 trenches etched only from the front side. A width of 50 µm per trench is realized by standard DRIE technique.

Results

In *Figure 1*, the SEM image of the MEMS structure indicates the extracted WLI measurement data. Automated WLI scans of MEMS structures spread across a 4" SOI-wafer are shown in *Figure 2*. Especially the data on the thin film thickness of the single crystalline silicon device layer displays the stated thickness variation of the wafer manufacturer of ±0.5 µm and gives a strong argument for the local knowledge of the device layer thickness for MEMS devices. Even more, a polycrystalline SiC thin film is analyzed with the same technique, and the thin film thickness, as well as the static deflection for two rows of devices, are shown in *Figure 3*. Following the considerations of Bao [7] on a beam under a bending moment, the residual stress values for the devices are calculated and shown in *Figure 4* as

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a function of the device position on the wafer, thus proving the high potential of this approach.

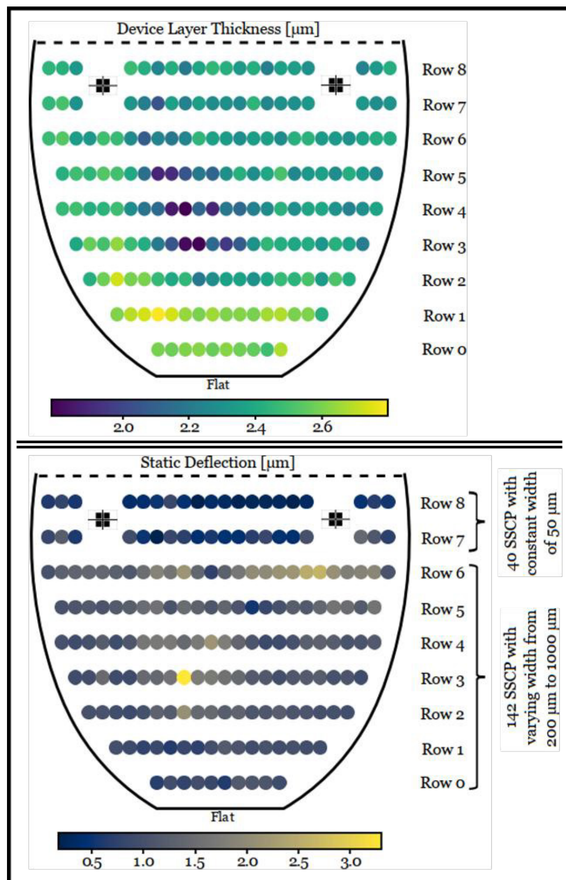

Figure 2: Scans of thin film thickness (top) and static deflection (bottom) on 182 MEMS structures positioned across half of the surface of a 4" wafer. The device layer material is single crystalline silicon from an SOI wafer with a stated thickness from the manufacturer of 2±0.5 µm. We find a rather large deviation in thin film thickness of 35 % but very low static deflection of the plates, resulting in low residual stress values below 10 MPa. The upper part of the wafer was used for investigations not relevant to this study.

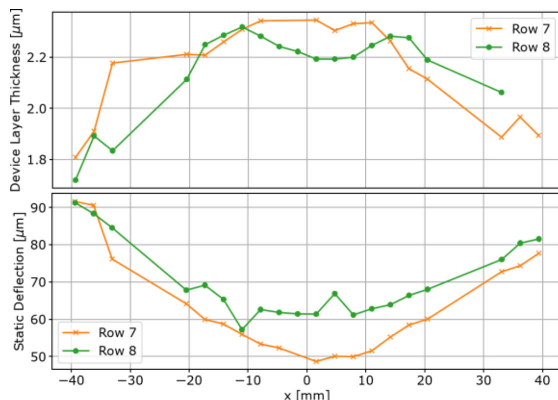

Figure 3: Local thin film thickness and static deflection of rows 7 and 8 across the center of a 4" wafer coated with polycrystalline SiC in an LPCVD process [8]. The wide spread of thin film thickness from 1.7 µm at the wafer edge to 2.3 µm in the center is expected due to the horizontal positioning of the wafer substrate in the quartz tube of the CVD furnace parallel to the gas flow.

The static deflection at the tip of the SSCP ranges from 50 µm in the center to 90 µm at the edge.

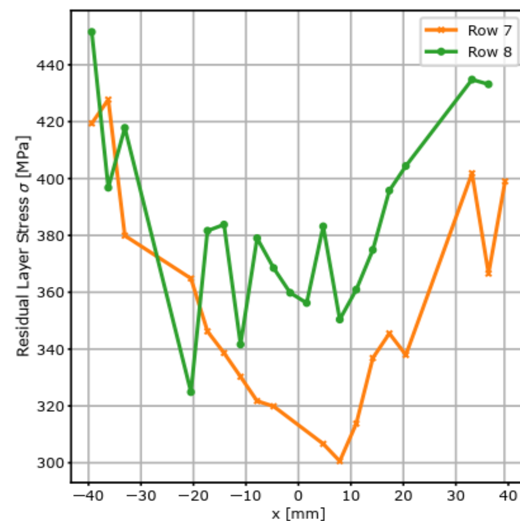

Figure 4: An experimentally determined Young's modulus of 217 GPa is used for the calculation of the residual stress for the measured SiC data in Figure 3, leading to a compressive stress in a range from 300 MPa to 450 MPa. Despite a reduction of the film thickness towards the edges of the wafer, there is an increase of the residual stress reflecting the increase of the static deflection of the SSCPs.

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