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Hierarchical Digital Offset Voltage Trimming of Fully-Differential Amplifiers in Self-X Sensor Electronics

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Summary:
This paper presents an improved approach to the digital offset voltage calibration scheme of fully differential amplifiers by splitting the adaptation process into two levels using separated coarse and fine digital-to-analog (DAC) current steering converters. The key feature is to avoid the matching complexity of using a single high-resolution DAC. Furthermore, the dynamic offset trimming process can be repeated based on the second DAC only, leading to a reduction in the calibration time. The achieved results based on Monte Carlo simulation show the ability to calibrate the offset voltage of the fully-differential instrumentation amplifier (In-Amp) below 100 µV for tackling offset voltage around ± 9 mV. The circuit is designed using XFAB 0.35 µm technology and verified with Cadence Virtuoso tools.

Keywords: Infield optimization, Self-X properties, Instrumentation amplifier, digital offset calibration.

Background, Motivation and Objective

The presence of the input offset voltage (V_{OS}) defines the amplifier resolution for detecting minimum input voltage in the sensor readout circuit. Furthermore, depending on the V_{OS} absolute value, it can drive the amplifier toward the output saturation region, thus reducing the output dynamic range when a high closed-loop gain is required. Several circuit-level solutions [1, 2, 3] are followed to tackle both the static and dynamic source of V_{OS} , avoiding the use of expensive and maybe not affordable wafer-level static approaches in the standard CMOS technology, e.g, laser trimming [4]. Digital offset trimming [5, 6] is a common dynamic technique owing to the advantages of simplicity and compatibility to the continuous- time signal processing circuits. However, the minimum V_{OS} is proportional to the resolution of the used digital-to-analogue converter. This abstract aims to use a higher resolution DAC with less matching constraints and to reduce the calibration time, which allows running the calibration period at a higher rate to support the principle of smart sensors with self-X properties (self-calibration, self-healing) [7,8].

Description of the Proposed Methodology

The block diagram of the proposed approach is depicted in Fig. 1. The calibration scheme is used to null the input offset voltage of the fully differential instrumentation amplifier (In-Amp) [9]. During the calibration time, the In-Amp is set to the maximum closed loop gain of 128 to subdivide the inherent offset voltage of the hysteresis comparator, while the In-Amp inputs are shorted to the common mode voltage (V_{CM}). Also, the configurable compensation capacitor is set to the minimum value to improve the settling time of the In-Amp without affecting the stability condition. The adaptation is split into two separate levels, in the first level a 6-bit segmented current steering (CS) DAC with 4-bit binary-weighted bits and 2 bits with thermometer coding to improve the matching on the top two MSB bits. In the second level, an 8-bit M3M CS DAC [10] is employed to fine-tune the VOS outcome from the first level.

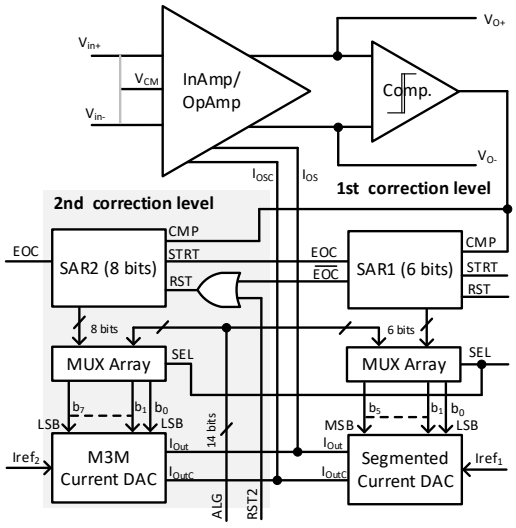

Fig. 1. Block diagram of the proposed digital V_{OS} calibration.

The two separated DACs do not need to match together as compared to a single 14-bit DAC.

Nevertheless, with this scheme, it is possible to iterate the calibration using the second level only, reducing the calibration time when tackling dynamic V_{OS} drift due to temperature and supply voltage fluctuations. Whilst both levels are only required at the chip startup. To enhance the calibration flexibility when used in smart sensory electronic systems, the inputs to the DACs are multiplexed to allow reading calibration data from the optimization algorithm performed on the digital-processing unit, which allows for infield adaptation concurrently during the measurement operation.

Results

To verify the circuit performance, both the In-Amp and the calibration circuit are simulated together to extract the V_{OS} using Monte Carlo (MC) with a large number of samples (1000 samples) per temperature and supply voltage corners (V_{DD}=3.3±10%, -40 ≤ T ≤ 85 ºC). This is important to count the offset voltage due to the DACs output currents mismatches and the residual offset of the comparator. The process variation of 6 σ with Gaussian distribution MC type is selected to emulate more realistic conditions of device fabrication. The worst-case result is found at T=-40 ºC and V_{DD}=3 V. Then the MC is again repeated with 1000 sample around the last corner to have a dense distribution at the worst corner. As shown in Fig. 2, most of the samples fall between V_{OS} = ± 9 mV with a steady deviation of 2.623 mV from the typical mean value.

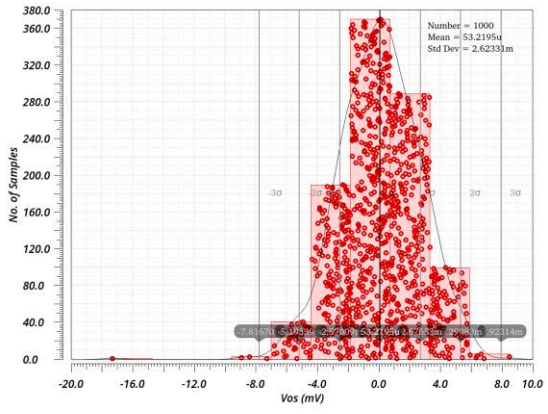

Fig. 2. MC simulation result at the worst-case corner.

The two maximum absolute V_{OS} is back annotated as a statistical corner from the MC sample batch to run the optimization scheme over it in the next step. Fig. 3 demonstrates how the calibrated V_{OS} is reduced below 100 µV in either case. A clock frequency of 100 kHz is used in this simulation test to drive the successive approximation registers (SAR). The estimated design area is 0.75 mm^2 and the power consumption of the optimization loop is about 140 µW.

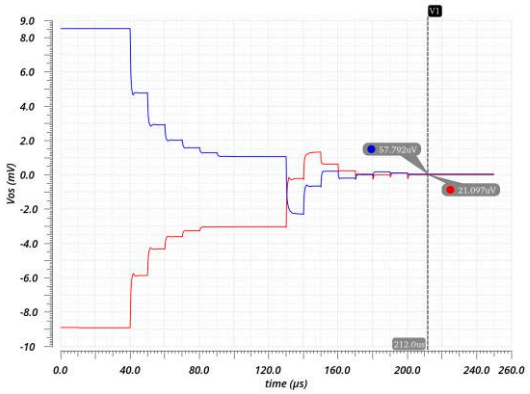

Fig. 3. Optimization run against maximum absolute extracted V_{OS} .

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