DOI 10.5162/SMSI2023/E6.4

Biological Neural Coding for Adaptive Spiking Analog to Digital Conversion

Hamam Abd[1], Andreas König[1]
[1] Institute of Cognitive Integrated Sensor Systems (KISE), TU Kaiserslautern Deutschland,
abd@eit.uni-kl.de

Summary:
A conventional ADC in leading-edge integration technologies faces numerous challenges due to manufacturing deviations, signal swings, noise, etc. Designers of ADCs are shifting to the time domain and digital design techniques to manage these challenges. Consequently, we aim to design a novel self-adaptive spiking neural ADC (SN-ADC) with promising properties, e.g., low-voltage operation, technology scaling issues, noise-robust conditioning, and low power. In this work, we focus on designing one building block of our concept, a decoder that converts place coding to digital code.

Keywords: Spike-domain information presentation, Biological neural coding, Industry 4.0.

Background, Motivation and Objective

The number and diversity of sensors increase with the progress in integration technologies due to the rapid progress of machine learning and artificial intelligence in the internet of things (IoT) and Industry 4.0 [1]. The performance of the smart sensor faces many problems due to dynamic and static divergence. These problems are effectively addressed by utilizing reconfigurable structures with self-X (self-optimization, self-monitoring, self-calibration, and self-healing) properties [2]. However, reconfigurable structures use amplitude representation that faces problems with leading-edge technologies. These advocates transition to spike domain representation with self-X properties.

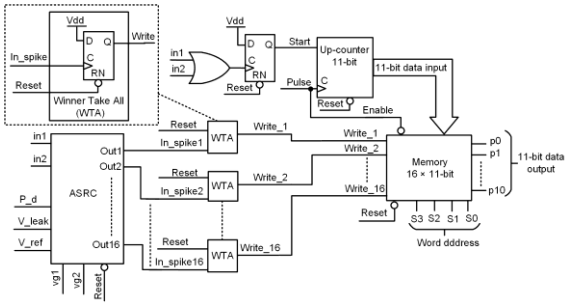

Fig. 1. Proposed schematic of place coding to digital code.

In our previous work, we proposed a self-adaptive spiking neural ADC (SN-ADC) system [1]. It is built on based rank order coding. It consumes a massive area and needs a high conversion time for the 14-bits. The required number of neurons and synapses is 16384 and 32768, respectively. Additionally, it needed 16384 cells of WTA. These advocated designing the SN-ADC based on another biological neural coding to decrease the consume area and increase the speed for the high resolution, e.g., 14-bits. Many coding schemes for biological neural transmission can be divided into density coding, rank order coding, and place coding [3]. In this work, we design a novel decoder that converts the place coding to digital code with promising features, e.g., high resolution, low area consumption, high speed, and low power consumption.

Proposed Methodology

In this work, we design a circuit that converts the place coding to a digital number (see Fig. 1). Every output of adaptive spike-to-rank coding (ASRC) is connected to one cell in the WTA circuit. The outputs of the WTA circuit are connected to the memory. There is a location in memory for each cell of WTA to save its place in the observation window. The outputs of the WTA write the counter output on their location on the memory when they convert from zero to one. The output of the OR gate is connected to the D-flip-flop clock, and flip-flop output is connected to the counter start. The counter is started increasing when the in1 or in2 input is presented. The 11-bit counter is used to divide the observation window into 2048 sub-windows. In our previous work [1], we designed the ASRC with 16 outputs. Therefore, in the current work, we implement memory with the 16 locations (see Fig. 2). Every location is set for one output of the ASRC to save its position. The proposed work needs 16 neurons and 32 synapses for the 14-bits. It used 16 cells of WTA. The proposed design is implemented using X-

FAB 0.35 µm CMOS technology and Cadence tools.

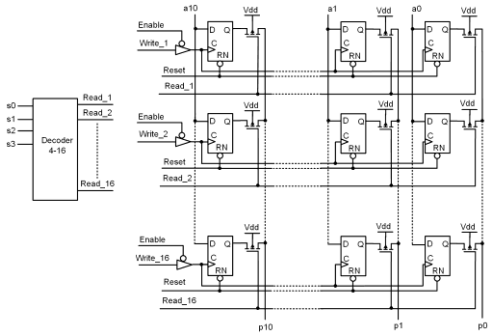

Fig. 2. Schematic of the memory.

Results

Figure 3 shows the ASRC outputs when two pulses are presented to the ASRC inputs with a difference of 3 ns between in1 and in2.

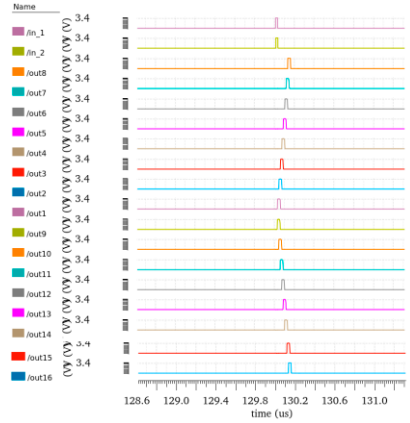

Fig. 3. Simulation of the ASRC, with a difference of 3 ns between in1 and in2

The ASRC outputs from out1 to out16 are shown in Figure 3 go to the inputs In_spike1 to In_spike16 of the WTA cells, respectively (see Fig. 1). The WTA cells generate pulses that are used to write the counter's output to the memory (see Fig. 4). The time difference steps between in1 and in2 are from −8044 to 8044 ns in steps of 1 ns, as shown in Table 1.

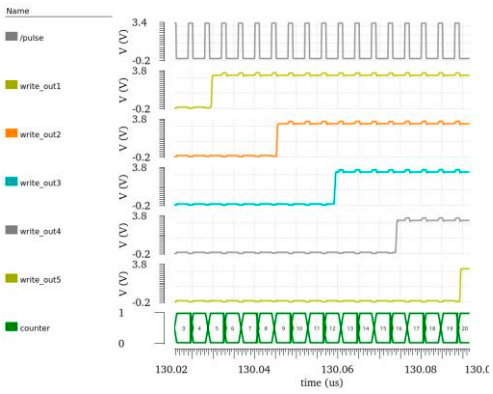

Fig. 4. Simulation of WTA outputs and counter,

Tab. 1: Place code outputs of the memory

In2-in1 (ns)	-8044	-8043	….	8043	8044
out1	5	5	….	2015	2016
out2	9	9	….	2020	2020
out3	13	13	….	2024	2025
out4	18	18	….	2028	2029
out5	22	22	….	2033	2033
out6	27	27	….	2037	2038
out7	31	31	….	2042	2042
out8	36	36	….	2046	2047
out9	2016	2015	….	5	5
out10	2020	2020	….	9	9
out11	2025	2024	….	14	14
out12	2029	2029	….	18	18
out13	2033	2033	….	22	22
out14	2038	2038	….	27	27
out15	2042	2042	….	31	31
out16	2047	2046	….	36	36

It obtains up to 16087 different output place codes representing 13.97 bits in the binary code. From the speed perspective, the conversion time is 8.142 us. From the energy consumption perspective, the energy consumption of circuits ASRC, WTA, counter, and memory is 103.3 pJ per 1 µs when there is no spike. They consume 1.24 nJ per spike when there is a spike. While in previous work [1], for 14-bit, the conversion time was 368.640 us, and the energy consumption was 91.56 nJ per 1 µs when there was no spike and 1.238 µJ per spike when there was a spike.

References

[1] H. Abd, and A. König. "Design of a CMOS memristor emulator-based, self-adaptive spiking analog-to-digital data conversion as the lowest level of a self-x hierarchy." Journal of Sensors and Sensor Systems https://doi.org/10.5194/jsss-11-233-2022,

[2] S. Alraho, Q. Zaman, H. Abd, and A. König.. "Integrated Sensor Electronic Front-Ends with Self-X Capabilities." Chips 1.2 (2022): https://doi.org/10.3390/chips1020008.

[3] S. Thorpe, A. Delorme, and R. Van Rullen. "Spike-based strategies for rapid processing." Neural networks 14.6-7 (2001): https://doi.org/10.1016/S0893-6080(01)00083-1.