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Optimization of Micro-Hotplates for better Performance as infrared Emitters

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Summary:
The optimization process for a particular application of micro-hotplates as infrared emitters is considered. It starts with a baseline combination of technology and design. This combination yields a set of 5 performance parameters (radiant flux, manufacturing costs, modulation speed, power efficiency, and device lifetime). Changes of design or technology often affect more than one parameter in an intricate way. Numerical simulations, which have been verified by experimental data, allow a prediction of the outcome of changes and thus a time and resource saving device optimization.

Keywords: membrane, microheater, micro-hotplate, infrared emitter.

Introduction

There is an increasing need for micro-hotplates in sensor applications. Those micro-hotplates can be used as infrared emitters [1] in gas sensors [2]. There are other kinds of infrared emitters which are based on semiconductor diodes of the AlInSb-system. By preparing quantum wells with these materials with thicknesses from 2 to 6 nm, it is even possible fabricate a LED with different emission wavelengths from 3.4 to 4.2 µm [3]. However, the band gap of the antimonides and the deposition technology limit the maximal attainable wavelength to less than 6 µm which compromises applications for infrared transmission sensing on organic molecules.

In this work we look at a set of performance parameters for micro-hotplate infrared emitters in the course to optimize for a certain sensor application. We consider a simply design change for enhancing the spectral flux in a desired spectral region and demonstrate the impact onto the performance parameters.

Basic Technology and Design

The start of an optimization is a baseline solution, which is a given manufacturing technology and a sensor design. As a substrate a double-side polished silicon wafer has been used. The most important part of such a device is its free-standing membrane which contains a heating layer which can be TiN, $MoSi_2$, or Pt sandwiched between dielectric layers such as silicon nitride, silicon carbide or silicon oxide. In the membrane area, the silicon is etched away, so that the membrane is only supported a its edge by the bulk silicon. An example (type A) is shown in fig. 1. The chip has edge dimensions of 1 mm x 1 mm, a circular membrane and a tapered heater in the middle.

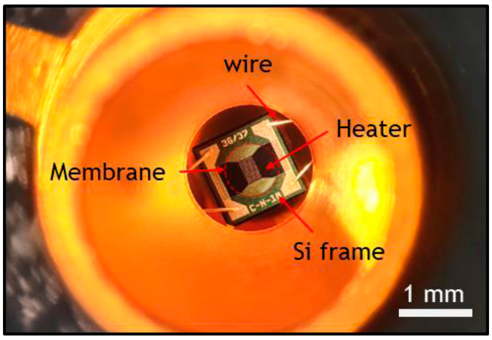

Fig. 1. Photograph of a micro-hotplate infrared emitter type A. The chip has been mounted and wire bonded on a transistor outline socket TO-39. On top of the socket a reflector cap has been placed to enhance the emission in forward direction.

Performance and Optimization Process

In order to discuss an optimization, we choose a set of performance parameters and give values for this chip. First of all, our presumed measurement task requires a certain spectral radiant intensity I_e at a wavelength of λ= 6 µm. Our type A emitter delivers I_e at λ = 6 µm of 0.24 mW/µm/sr. The costs of such a device are crucial in industrial applications. The chip manufacturing costs K vary approximately with the chip area. For the small type A chip, K is of the order of a few € per piece. K also scales with the number of produced parts. The next important parameter very often is the switching speed or the cutoff frequency f_c. We determined f_c by observing the radiant flux with a fast InAsSb photodiode while exciting the emitter with square wave electrical modulation and taking the frequency at a decay down to 63% of the static flux. For type A f_c is 51 Hz. Device reliability plays an important role, too. Our devices shall have a mean time to failure *MTTF* of several years. For some applications, for instance when powered by a field bus, energy efficiency η as the ratio between the total radiant flux and the electrical input power has to be considered. Because the edge of the membrane is very close to the heated zone, heat can dissipate fast to the silicon frame and further to the socket, our type A emitter has an η of 5.7%.

All of these parameters are an outcome of a particular technology and a particular design. Any changes in design or technology may likely cause changes in the performance parameters, which is symbolized by figure 2.

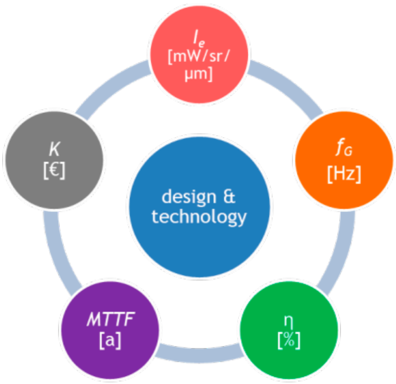

Fig. 2. The 5 main parameters of an infrared emitter are a result of a particular design and technology.

Increasing the radiant flux

For optimizing I_e of the type A emitter, several design or technology options are possible. The first very obvious one is to increase the emitting area, i.e. fabricate a larger chip, see figure 3. Compared to type A with 1 mm edge length, type B (2 mm) and C (3.6 mm) emit 4.7 times and 26 times more light at λ = 6 µm, with costs scaling by the chip area. The I_e increase scales above linearly with the membrane size, which is caused by a better thermal isolation between the heater and the silicon frame, increasing η to 6.3% and 19.3% !, respectively without much detrimental effect on the *MTTF*. On the other side, f_c decreases from 51 Hz down to 26 Hz and 7 Hz !, respectively.

Instead of measuring fabricated devices, with knowledge of the material parameters all three physical quantities I_e, f_c, and η can be calculated by numerical simulations. With a validated multiphysical model, this enables for a much faster optimization speed in comparison to experiments. Figure 4 shows one outcome of the electrical-thermal model for the type C emitter. The temperature distribution as well as temporal behavior were simulated by the model and are in close agreement to measurements.

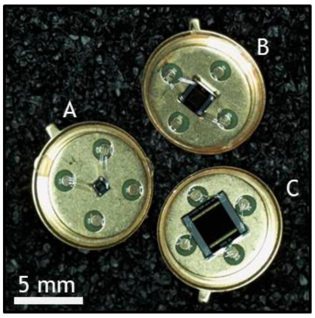

Fig. 3. Photograph of 3 chip types fabricated with similar technology.

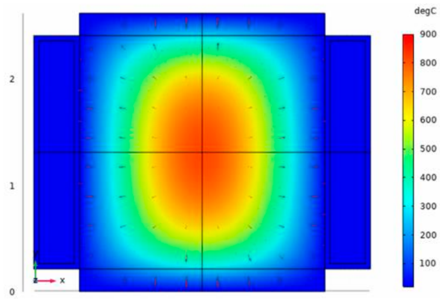

Fig. 4. Multiphysical thermal-electric simulation of the temperature distribution on the membrane of the type C emitter at 700 mW of electrical input power.

Summary

Changes of design or technology often affect more than one parameter in an intricate way. Numerical simulations, which have been verified by experiments, allow a time and resource saving device optimization.

Acknowledgments

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