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Electrical Characterization of the SiO_2/4H-SiC Interface

Chezhiyan Nanjappan[1], Georg Pfusterschmied[1], Ulrich Schmid[1]
[1] Institute of Sensor and Actuator Systems, Gußhausstraße 27-29, 1040 Wien, Austria,
Corresponding Author's e-mail address: chezhiyan.nanjappan@tuwien.ac.at

Summary:
The interface trap density D_{it} is an important parameter to characterize the quality of the oxide/semiconductor interface. The low channel mobility (20 cm^2/Vs for dry thermal oxidation) in silicon carbide-based MOS devices is mostly attributed to the high amount of interface traps. To attain high mobilities (>80 cm^2/Vs), it is required to reduce the D_{it} to the range of 10^{10} $cm^{-2}eV^{-1}$ or below. Post oxidation annealing under nitrogen-based gaseous environment is known to reduce D_{it}, but still there is the requirement to reduce the D_{it} to reach those values of standard silicon/silicon-dioxide interfaces (10^{10} – 10^{11} $cm^{-2}eV^{-1}$). Oxides on SiC formed by plasma oxidation process instead of dry oxidation represents a promising technology, as it is known for exhibiting lower D_{it} values in the range of 10^{10} – 10^{11} $cm^{-2}eV^{-1}$. However, the physics behind the plasma oxidation of 4H-SiC is not yet completely understood. In this work, we report first results about the enhanced oxidation rate and improved electrical characteristics when an oxygen plasma pre-treatment is implemented before the standard dry oxidation of 4H-SiC.

Keywords: Siliconcarbide, thermal oxidation, plasma oxidation, TEOS, interface, defect density.

Introduction

Hexagonal silicon carbide (4H-SiC) has gathered considerable interest in the recent decades due to its superior material properties compared to silicon (Si). The high band gap of 3.26 eV, a high thermal conductivity of 450 W/mK and a high breakdown field of 2.4 MV/cm makes this compound semiconductor a promising candidate especially for power electronics. A bottleneck of SiC-based devices is the low inversion channel mobility (n-channel mobility ~40 cm^2/Vs for TEOS deposited oxide), while their Si counterparts exhibiting a mobility of ~360 cm^2/Vs [1-3].

Dry thermal oxidation is the most widely used method for the oxidation of SiC. On the SiC surface, oxygen reacts with silicon and forms amorphous SiO_2 at temperatures above 1000°C. The remaining carbon from the SiC crystal lattice either outgasses as carbon oxides (CO or CO_2) or remains in the oxide or at the interface as structural defects (SiO_xC_y) [4]. As the latter are electronically active, SiO_xC_y species are regarded to reduce substantially both the oxide quality and the transition region at the interface, thus negatively impacting the channel mobility. Moreover, it is a time-consuming process (for example, obtaining 100 nm thermal oxide on the Si-face of 4H-SiC it takes about 20 hours at 1200°C [5]) with the requirement of a high thermal budget [4-8].

Plasma oxidation on SiC is facilitated by exposing the substrate to highly active oxygen plasma. Compared to dry thermal oxides, plasma oxides have reduced concentration of the carbon species (SiO_xC_y) because the highly active oxygen atoms (O_2^*) react with these carbon species to form SiO_2 and CO or CO_2 is outgassed as shown in eq. (1). This results in a reduced number of the interface state density D_{it} (10^{10} – 10^{11} $cm^{-2}eV^{-1}$) compared to dry oxidation with D_{it} values in the range of 10^{12} – 10^{14} $cm^{-2}eV^{-1}$ [3, 4].

$$SiO_xC_y + O_2^*(\text{plasma}) \rightarrow SiO_2 + CO(g)/CO_2(g) \quad (1)$$

In plasma oxidation, it is the diffusion of high active oxygen atoms (O_2^*) through the interface while in thermal oxidation it is mostly O_2 molecule that migrate to the SiC/SiO_2 interface [4].

Another technique of oxide formation on SiC is oxide deposition from tetraethyl orthosilicate (TEOS). A bubbler-system in combination with argon (Ar) as carrier gas is used to hydrolyze TEOS. The hydrolyzed TEOS-Ar gas mixture is introduced to a process chamber where SiO_2 is deposited on the SiC substrate at low pressure levels of < 1 Torr and temperatures of about 700°C. Since this technique does not consume the substrate, there is no incorporation of carbon atoms into the oxide or any accumulation of carbon at the interface (D_{it} -10^{11} -10^{12} $cm^{-2}eV^{-1}$) [3]. Also, the deposition rate is high (~15 nm min^{-1}) compared to the previous methods and does not show any thickness dependencies. Main drawback of TEOS oxides is that they suffer from

increased gate leakage, which is likely due to the presence of structural defects and trapped charges originating from dangling bonds predominantly at the interface [3, 11].

Experimental details

MOS capacitors were fabricated with commercial n-type 4H-SiC substrates with a 5 µm thick epilayer on top. The doping concentration of the epilayer was ~$2 \cdot 10^{16}$ cm^{-3}. Wafer was first cut into 1 cm x 1 cm squared sample snippets. All samples were cleaned using standard RCA (Radio Corporation of America) cleaning procedure before further processing.

For this study three samples have been investigated. Sample #1 was thermally oxidized at 1100°C in pure O_2 atmosphere at 760 Torr pressure for 34 hours. Sample #2 was pre-treated with an oxygen plasma before thermal oxidation (same process as sample #1). On sample #3 the oxide layer was deposited using TEOS. The fabrication of sample #3 was conducted by an external service provider and can be considered as an industry reference standard. A SiO_2 layer thickness of around 100 nm was achieved on all three samples. Next all samples underwent post oxidation annealing in nitrous oxide (N_2O) environment at 1100°C which facilitates nitridation of the interface, thereby reducing D_{it}.

For electrical characterization, Titanium (Ti) and Platinum (Pt) were sputtered on the bottom sides of the substrate. Then the samples were subjected to rapid thermal annealing at 1000°C for 1 minute to obtain a good ohmic contact. Aluminum (Al) was evaporated for the gate electrode. An array of circular metal pads with a diameter of 500 µm are patterned by wet etching.

Results

The oxide thickness of sample #1, #2 and #3 were 118 nm, 135 nm and 100 nm, showing that the enhanced oxidation rate during thermal oxidation by about 14 % when plasma pre-treatment was applied. The oxide layers were characterized using AFM, SEM and TEM.

Capacitance-voltage (C-V) and conductance-voltage (G-V) measurements were done simultaneously to evaluate the quality of the MOS capacitors. From C-V curves, the doping concentration (Sample #1 and #2 - $8.1 \cdot 10^{16}$ cm^{-3}, #3 – $1 \cdot 10^{16}$ cm^{-3}) of the epi layer was obtained by plotting $1/C^2$ vs V. From G-V measurement, the flatband voltage (Sample #1 – 3.4 V, #2 – 0.4 V, #3 – 0.9 V) was obtained. Next, the ideal CV curve was calculated with the determined flatband voltage and doping concentration. Then the D_{it} is calculated with the Terman method [10].

From the results (see Fig. 1), we can clearly see that the plasma pre-treatment reduces the D_{it}, but needs further research efforts to reach the industry standard D_{it} values from TEOS oxides on 4H-SiC.

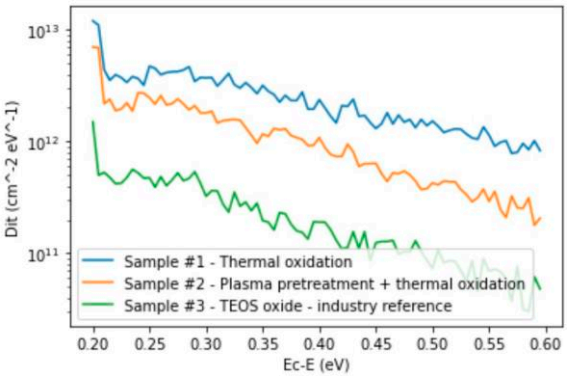

Fig. 1. Interface state density values of industry reference TEOS oxide, thermal oxide and plasma pretreated thermal oxide.

Conclusion

We investigated thermal oxidation on 4H-SiC substrate with an additional plasma pre-treatment step. We observed that the plasma pretreatment results in increased oxide rate and also improves the electrical properties of the MOS capacitor. In the near future, the reason for this improved oxide quality when applying this plasma pretreatment has to be studied, so that better quality oxides can be fabricated with this approach.

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