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Detecting Local Delamination of Power Electronic Devices through Thermal-Mechanical Analysis

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Abstract:
Die attachment delamination is one of the most common defects that happen over the life-time of a power electronic module [1]. It is usually the consequence of thermal mechanical stress that occurs during active operation of the device due to CTE (coefficient of thermal expansion) mismatch of its components. Additionally, even during the production cycles, errors can emerge, where the chip is not fully attached to the substrate. This can lead to premature failure of the final product. Aim of this paper is the detection of local delamination spots through pre-existing optical techniques. This novel non-destructive method will allow the isolation of defective devices during production or warn the overall system during operation, if a failure is imminent.

Keywords: Power electronics, Reliability, Non-destructive testing, Thermal-Mechanical Analysis, Die attachment

Optical Measurement Methods

Thermal-Mechanical stress in a power module will result into warpage of the system. One way to observe this deformation is by using the Digital Image Correlation (DIC). Here, the sample is first prepared with a stochastic black and white pattern. Two high resolution cameras observe the movement of the black dots during heating and calculate the stress and strain by comparing the reference image taken at the start of the measurement with subsequent images shot [2].

Another way to measure the deformation is by using the Electronic Speckle-Pattern Interferometry (ESPI) (Fig. 1). In this method, a continuous laser is used to illuminate the measurement area constantly. The Interference between reference and measurement beam will provide phase information that is used to calculate the result.

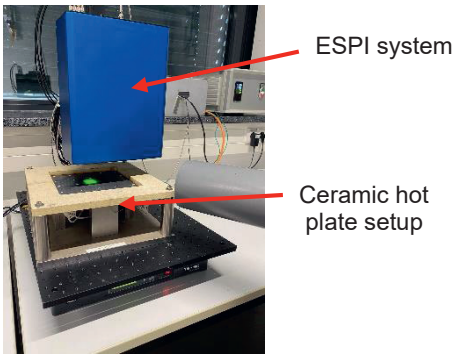

Fig. 1. Measurement setup for ESPI during passive heating.

Modelling of Delamination Effects

The main focus of this paper are IGBTs (Insulated Gate Bipolar Transistors) and power diodes. Samples with intentionally built in defects are manufactured with an established silver sintering process on top of PCB substrates (Fig. 2) [3]. During the step of printing the SnAg paste on the PCB with a stencil, we use custom made stencils with smaller openings compared to the regular process. By varying the geometry of the openings, we can produce chips that are not attached to the substrate at specific locations. Thus, we achieve samples that model the delamination process perfectly. Finally, the deformation is captured with the help of DIC and ESPI systems. Through comparing the warpage of healthy and defective samples, we want to correlate the behavior of the deformation with the magnitude and location of the defect. FE-simulation of samples with varying sinter layers are created to serve as a base for comparison for the measurements.

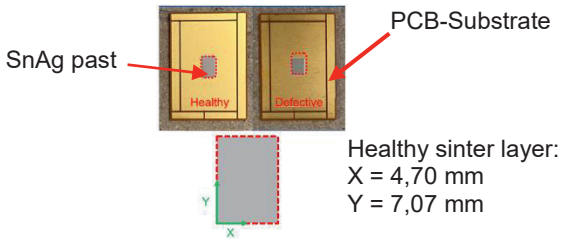

fig. 2. IGBT samples with healthy and defective sinter layers through variation of their x and y value.

Results

Simulation results for the warpage of an IGBT chip with a reduced length in Y-direction of 5,57 mm at increased temperatures show significant overshoot in the area of local delamination. (Fig. 3).

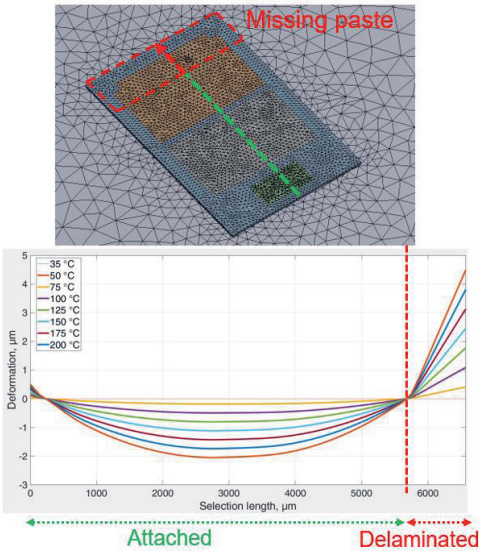

Fig. 3. FE-simulation of delamination effects with Ansys Workbench.

This behavior is to be compared to the measurement results with DIC and ESPI. A phase image taken with the ESPI already shows the area of delamination clearly (Fig. 4).

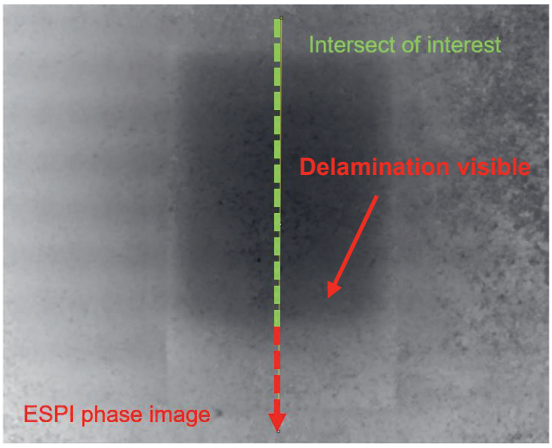

Fig. 4. ESPI phase image of IGBT with delamination.

It is notable that the same overshoot behavior seen in the simulation can also be found in the measurements. Comparing the simulation (Fig. 4) with the DIC and ESPI results (Fig. 5 and Fig. 6), one can clearly see that the delamination starts at a section length of about 5,5 mm, which matches with the new length in Y-direction of the sinter layer. The graphs also show that the ESPI provide much better results with less noise.

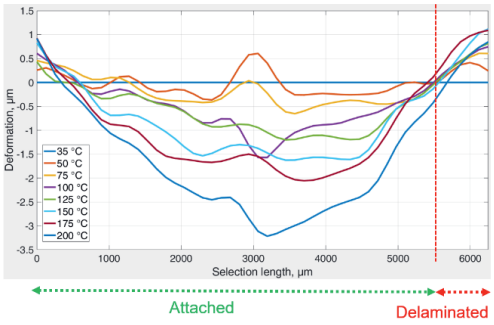

Fig. 5. Deformation along IGBT chip at various temperatures monitored with DIC.

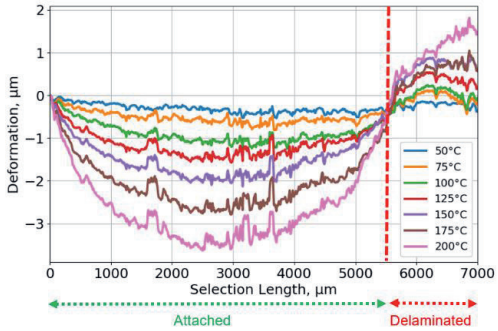

Fig 6. Deformation along IGBT chip at various temperatures monitored with ESPI.

Conclusion

In this paper, we have proposed a novel non-destructive method to test power electronic devices of delamination defects by performing a thermal-mechanical analysis. For this purpose, an established sinter process is varied to allow the user to intentionally create locations of low attachment between chip and substrate. Following, the warpage of healthy and defective samples during passive heating on a hot plate are recorded with optical methods and compared. This shows that locations of delamination show characteristic behaviors in their warpage, which can be used as an indication for fault detection.

References

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