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Predicting the Analog Integrated Circuit Performance Using Indirect Measurements Based on Simulations

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Summary:
This paper presents a low-cost indirect measurement method to predict the performance of analog integrated circuits (ICs). The method is based on integrating simple sensors near to the main circuit to capture circuit properties under different conditions expected by real fabrication. Monte Carlo with corner simulation results is used to train neural network for modeling and mapping the sensor outputs to the design output performance. The achieved correlation performance metrics is 91.68%. The circuit is designed using AMS 0.35 µm technology and Cadence tools.

Keywords: Neural Network, Artificial Intelligence, Indirect Measurements, Non-intrusive sensors.

Background, Motivation an Objective

The merging of AI and ML with other developing technologies, such as industrial internet of things I(i)OT and cyber-physical production systems (CPPS) is empowering the significant revolution in the industrial domain [1] known as industrial 4.0 [2]. In industry 4.0 and IoTs devices, smart integrated sensors perform a central role in data generation [1]. Normally the performance of smart sensory electronics (SSE) is decayed with the passage of time [3]. To address the aging and process variations effects, commonly, analog ICs are overdesigned, that leads to consume more power and or larger chip area. Nevertheless, ML in SSE will enable the self-x (self-optimize, self-calibration, self-healing, etc.) properties [4]. One of the primary calibration methods is designing the analog ICs with controllable tuning knobs and performance measurement set-up [5] for chip performance monitoring [6]. So, the main objective in this research work is to find out a cost-effective indirect performance evaluation method (IMs) for SSE toward reducing the number of real expensive chip measurements.

Proposed Methodology

The block diagram of the proposed IMs is presented in Fig. 1, the non-intrusive sensors (NS) are integrated on chip in close proximity to the main design under test (DUT) to face the same conditions imposed on the DUT, that is PVT variations (process, voltage, temperature). An artificial neural network (ANN) is used to map NS and DUT performance and creates accurate regression model to indirectly and more easily predict DUT performance based on the sensors data. The flow diagram of the proposed measurement approach is depicted in Fig. 2.

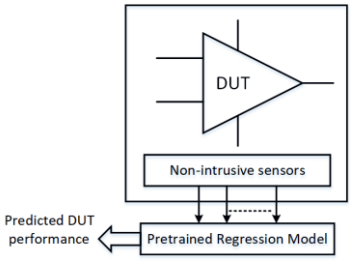

Fig. 1: Block diagram of the proposed IMs method

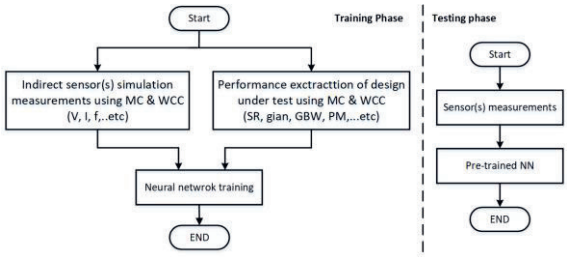

Fig. 2: Flow chart of the proposed IMs methodology

During training phase, both DUT and NS are simulated and subjected to the same PVT condition using combination of worse case corners (WCC) and Monte Carlo (MC) with enough samples (200 samples) to accurately capture real fabrication process profile. 80% of data samples are randomly selected to train the ANN while the remaining 20% are used to evaluate its performance. In the testing phase, the data provided by NS to the pre-trained ANN is used to indirectly predict the DUT performance.

A single-ended operational amplifier is used as DUT in this experiment to verify the proposed

concept. The measurements quantities of the DUT are slew rate, DC gain, gain-bandwidth product, and phase margin. The remaining simple characteristics are left for the real measurement because it will consume considerable time during simulation. A feasible solution is to increase computational resources to cover more tests by simulation. The clock generator based on ring oscillator (RO) circuit shown in Fig. 3 is designed as PVT monitoring circuit.

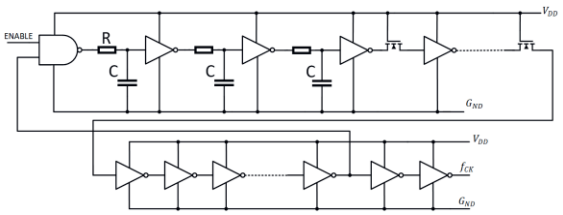

Figure 3: Ring oscillator for process monitoring.

RO shares almost the same circuit devices of the DUT to increase data correlation between both and thus improving the ANN modelling and prediction accuracy. The first test result shows weak prediction level of the ANN with adjusted R squared value (ARS) of 30.48%. It concludes that although RO alone is showing good sensitivity to the PVT variations, however, its performance is mostly dominated by RC components, thus not providing enough correlation information with the DUT to the ANN. Hence, additional NS with different sensitivities to PVT is required to further enhance ANN modelling. Authors in [7] presented a circuit to monitor the transistors threshold voltage (Vth) variation with the process by reading the voltage drop on PMOS diode connected transistor working in the weak inversion. Though, we count that is not enough to monitor Vth of PMOS only while the NMOS can go in opposite process corner. Hence, we proposed a modified version of this circuit as shown in Fig. 4 to monitor both of NMOS and PMOS Vth variations.

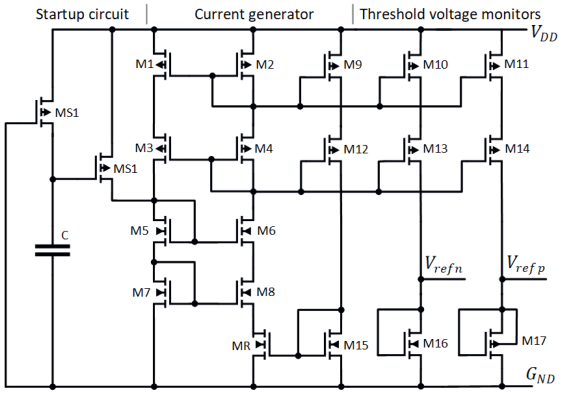

Figure 4: Threshold voltage monitor circuit.

The resistor-less current biasing circuit [8] is used to generate reference current insensitive to supply voltage and has small positive temperature coefficient. All transistors in the circuit work in the subthreshold region, except for MR that is in the triode region functioning as MOS resistor. By including PMOS threshold voltage readings from Vrefp together with the RO frequency data, the measurement prediction is improved with ARS of 70.5%. In the last experiment the Vrefn data is added and the prediction accuracy improved significantly with ARS equal to 91.68%. The performance of the proposed methodology is illustrated graphically in Fig. 5. In the future, we are working to have all types of NS outputs in digital form to have more immune outputs to the observer noise.

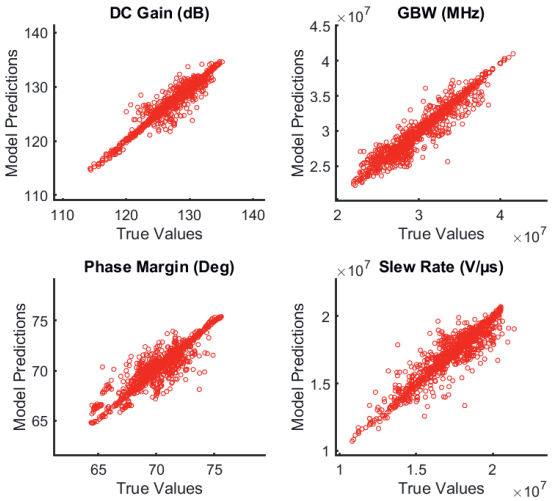

Figure 5: Scatter plot of the predicted and true values.

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