Ultra-thin resistors for piezoresistive sensors

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Abstract

Different ion implantation techniques for the fabrication of shallow boron doped layers used as piezoresistors have been evaluated. In the present case the corresponding process parameters have been optimized to meet demands for high deflection sensitivity of piezoresistive AFM cantilevers. Boron doped layers with decreased pn-junction depths down to ~ 20 nm has been fabricated showing increased deflection sensitivities of $(10\text{-}20)\cdot 10^{6}\ \Omega\cdot m^{-1}$ compared to conventional implanted resistors. The used ion beam technique fulfils requirements for pn-junctions in terms of small junction depth and low sheet resistance. Additionally, the piezoresistor fabrication processes was evaluated in combination with other ion implanted elements integrated in AFM cantilevers.

1. Introduction

Piezoresistors in silicon has found applications in different kinds of sensors, for example in pressure sensors, accelerometers, multi-axis flow sensors and tactile sensor arrays. The emerging use of piezoresistive elements for deflection sensing of scanning probe cantilevers in Atomic Force Microscopy (AFM) is governed by efforts to overcome limited speed imaging by video rate imaging [1] and throughput using monolithically integrated arrays of AFM cantilevers [2-4]. Consequently, to the integration of the detecting piezoresistive sensor, electro-thermal actuator integration into the cantilever compatible with modern CMOS processing has to be considered as fundamental for the realization of fast and large area high-resolution imaging.

However, having a large number of micro-cantilevers in the array requires integrated deflection sensing schemes, such as piezoresistive sensing [5]. Among them, piezoresistive sensing has been widely used mainly because of the high sensitivity and ease of fabrication and implementation. Piezoresistive sensing has been shown to be very sensitive with sub-nanometer minimum detectable deflection [6] and can be used in both static and dynamic modes for sensing. Moreover, in an AFM under feedback control, each cantilever has to be individually addressable in the z-direction. Integrated actuators can achieve feedback actuation and self-excitation of the cantilever. Among thermal bimorph actuators to deflect the cantilever [7,8] thermo-mechanical actuation using doped single crystal heater elements integrated into the cantilever seems to be one of the best choice. Consequently, to the integration of the detecting piezoresistive sensor, electro-thermal actuator integration into the cantilever compatible with modern CMOS processing has to be considered as fundamental for the realization of fast, high-resolution imaging by using massively integrated PRONANO AFM arrays [7]. With shrinking of piezoresistive sensor dimensions in general and piezoresisitive cantilevers in AFM arrays (Si membrane or cantilever thickness < 2 µm) the reduction of the resistor thickness (small pn-junction depth) in correlation with a desired resistance becomes more and more important.

As an example, the contribution describes mainly the fabrication of p-type silicon piezoresistive sensing and shortly of actuating resistive heater elements integrated in AFM cantilever arrays using ion implantation for doping of all elements including corresponding interconnecting lines between them. Because it has been predicted that for p-type piezoresistivity the values of the piezoresistive coefficients in ultra-shallow boron doped layers with a pn-junction depth < 10 nm can be approximately two times higher than in the p-type silicon bulk material [8] special efforts are done for the realization of ultra-shallow boron profiles using different kinds of ion beam processing. The deflection sensitivity of selected ultrathin resistors has been measured and compared with conventional p-type silicon resistors. Finally, technological challenges and problems at ultra-thin resistor fabrication and their integration in piezoresistive silicon sensors are shortly discussed.

2. Device structure and fabrication

As an example the fabrication and investigation of ion implanted ultra-thin resistors will be described for the application of piezoresistive deflection sensing in AFM cantilevers. The device of an individual cantilever from the massively integrated PRONANO AFM array [7] with integrated piezoresistor and heater fabricated on Silicon-On-Insulator (SOI) wafers with Electrical-Through-Wafer-Interconnects (ETWI) is schematically shown in Fig. 1.

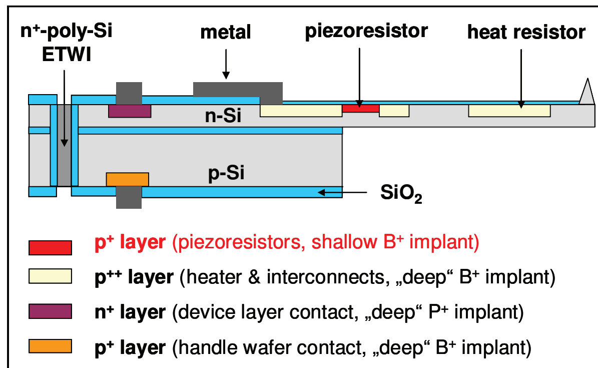

Fig. 1:
Schematic cross-section of a PRONANO AFM cantilever with integrated piezoresistor and heater fabricated on Silicon-On-Insulator (SOI) wafers with Electrical-Through-Wafer-Interconnects (ETWI)

As can be seen for full processing of PRONANO AFM arrays three different kinds of doped areas in the 2 µm thick device layer on the front side and one doped area in the handle wafer on the back side must be fabricated. This means that four ion implantation steps are necessary:
(i) shallow boron (B^+) implant for piezoresistor formation,
(ii) boron (B^+) implant for heater and interconnect line fabrication,
(iii) phosphorous (P^+) implant for contact formation to the n-type device layer and
(iv) boron implantation (B^+) for contact formation to the p-type handle wafer.

The most important and critical ion implantation step is the shallow boron implant for the fabrication of piezoresistors with defined sheet resistance in the n-type device layer of the SOI substrate. The boron implant of the heater can be carried out together with implantation doping of the interconnect lines from the piezoresistors and heater to corresponding electrical contact pads. Additional P^+ and B^+ implantations are necessary for contacting and reverse-biasing of the n-type device layer and the p-type handle substrate of the SOI wafer, respectively. Resistivities and related electrical characteristics (pn-junction leakage currents and breakdown voltages) of processed resistors were measured on test fields for the piezoresistors. Using these test structures resistance measurements on all boron implanted pn-junctions (piezoresistors, p^{++}-heaters, p^{++}-interconnects) have been carried out independently. Parallel to the experimental work simulations of boron profiles were done and applied to selected process parameters. For the simulation of the as-implanted boron profiles the CRYSTAL-TRIM code [9] was used and the profiles after annealing were simulated applying the TESIM code [10]. Simulated boron profiles have been compared to profiles measured by Secondary Ion Mass Spectrometry (SIMS).

3. Shallow boron doped piezoresistors

For the fabrication of shallow boron doped pn-junctions (piezoresistors) two techniques have been evaluated: (i) low energy implantation of 1 keV B^+ ions without pre-amorphization, and, (ii) ultra-shallow junction formation using point defect engineering (PDE) [11,12].
At low energy implantation different process parameters of the B^+-implantation and annealing conditions were investigated. Fig. 3 shows the results of the measured SIMS profiles in comparison with simulated profiles using the TESIM code. As can be seen, the depth of the pn-junctions x_j of the piezoresistors is located at about 70, 100 and 160 nm for annealing times 10, 30 and 60 s at 1000 °C, respectively.
The measured and simulated boron profiles are in good agreement. According to published data it must be taken into account, that at 1000 °C the electrical activation of boron is only 20, 25 and 40 % of the implanted dose for RTA annealing times of 10, 30 and 60 s, respectively. To meet the desired resistance of 2 kΩ of the piezoresistors an implantation of 1 keV B^+ ions at a dose of $1x10^{15}$ cm^{-2} and an annealing time of 60 s at 1000 °C were selected as optimal conditions. The sheet resistance (Fig. 4) of the piezoresistor area was measured as 270 Ω/square for t_1 = 30 s and 225 Ω/square for t_2 = 60 s, so the fabrication of the piezoresistors will employ a RTA for 60 s.
For further decreasing of the pn-junction depth x_j below 50 nm the process of ultra-shallow junction formation using point defect engineering (PDE) has been investigated. The wafers were irradiated by Si^+

ions of E = 400 keV with three doses of $D_1 = 1x10^{14}$ cm^{-2}, $D_2 = 5x10^{14}$ cm^{-2} and $D_3 = 1x10^{15}$ cm^{-2} to create appropriate defect distributions in the sample (accumulation of vacancies in the near surface region).

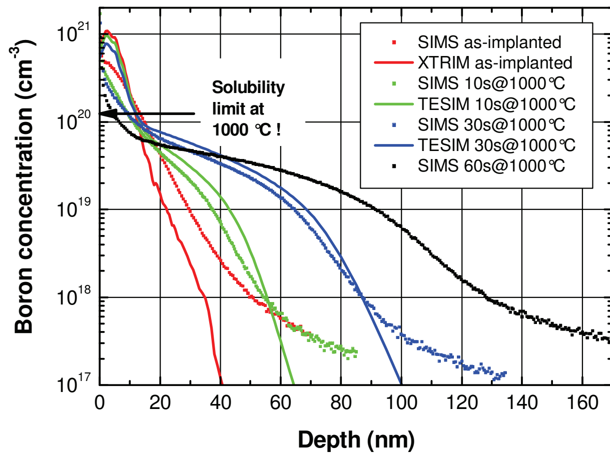

Fig. 3:
Boron SIMS profiles (solid lines) in comparison with simulated profiles (dashed lines) using the TESIM code for 1 keV B^+ implantation and RTA annealing at 1000 °C for 10, 30 and 60 s.

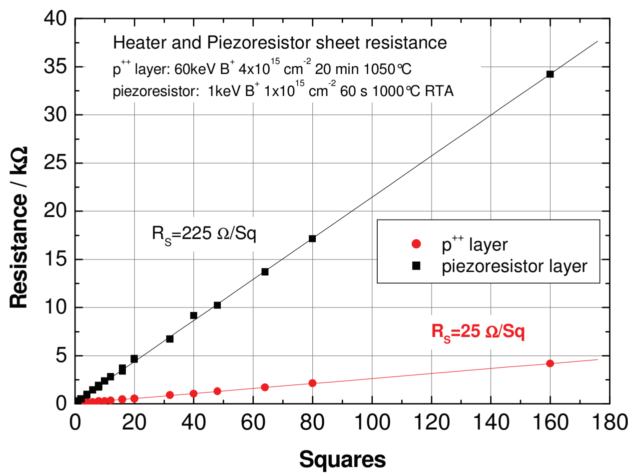

Fig. 4:
Determination of the sheet resistances for the piezoresistors and p^{++} heater and interconnect layers by plotting the line resistance vs. line length.

After that a boron layer of 10 nm thickness was deposited onto the wafers by thermal evaporation and the samples were subsequently annealed by RTA for 10 s at T_1 = 900 °C, T_2 = 950 °C and T_3 = 1000 °C for each Si^+ ion dose. Afterwards the remaining boron layer was removed by etching in hot nitric acid. SIMS measurements were used to investigate the boron distribution in the samples and the boron removal. Measurement results in Fig. 5 show that the diffusion depth (transient enhanced diffusion, TED) can be significantly decreased by high energy Si^+ implantation prior to the RTA treatment, which is suitable for ultra-shallow junction formation with junction depths x_j in the order of 20 – 40 nm. Such shallow junctions are necessary if the AFM cantilever thickness will be further reduced in the future and to achieve higher deflection sensitivities of the piezoresistors.

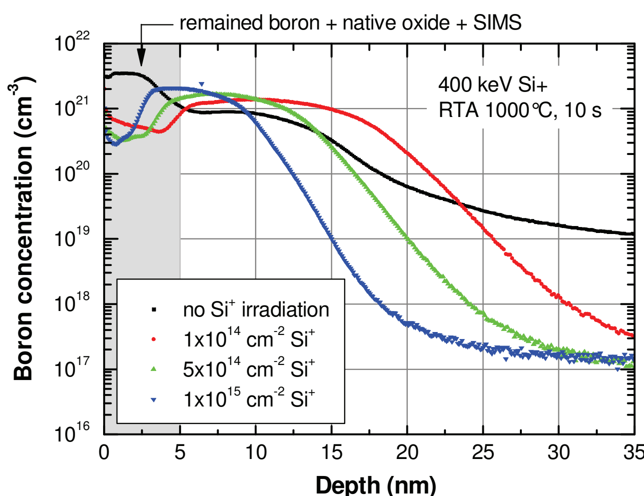

Fig. 5:
Boron depth profiles measured by SIMS on processed samples applying point defect engineering (PDE).

The sheet resistance for the boron doped piezoresistor layers fabricated using Point Defect Engineering (400 keV Si^+ ions), followed by in-diffusion from a deposited boron layer by RTA (10 s, 1000 °C) has been measured and is in the range of 170-200 Ω/square. The lower sheet resistance of the piezoresistors compared to 1 keV B^+ implantation can be easily optimized by varying the annealing conditions to meet the desired resistance values of the piezoresistors.
For selected samples implanted with 1 keV B^+ ions additional investigations of charge carrier depth profiles were carried out. For this purpose, the Stepwise Oxidation Profiling technique (SWOP) [13] was applied. The procedure works by altering between electrical sheet resistance measurements and Si consumption by electrochemical anodic oxidation. The carrier depth profiling was done using planar van-der-Pauw (VdP) structures. It was shown that the SWOP profiles are matching very well with SIMS reference measurements, and a depth resolution of ≤ 1 nm and a detection limit of $1{\cdot}10^{16}cm^{-3}$ was achieved [14]. As an example, Fig. 6 shows the carrier concentration depth profiles for 1 keV B^+ implanted planar VdP samples RTA annealed at 1000 °C. The plot consists of one profile for each RTA time of 10 s, 30 s and 60 s and the corresponding SIMS reference profiles.

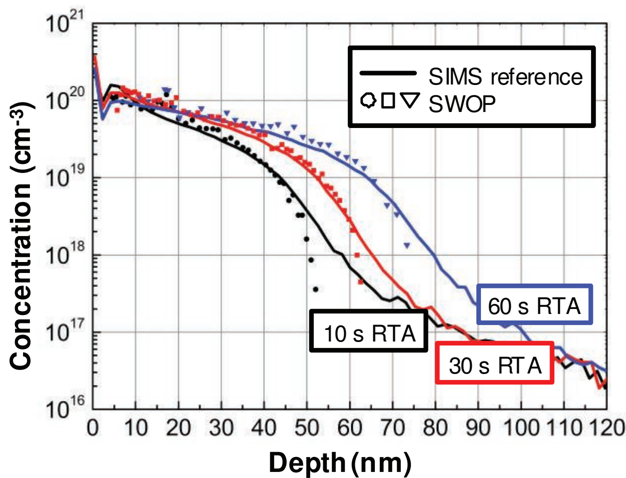

Fig. 6:
Charge carrier profiles and boron SIMS reference profiles for B^+ implantation 1 keV, $3{\cdot}10^{14}$ cm^{-2}, RTA annealed at 1000 °C.

It has to be mentioned that for the investigation of the charge carrier profiles (and the boron activation) the B^+ ion dose was lowered from $1x10^{15}$ to $3x10^{14}$ cm^{-2} to be in the solubility limit of boron in Si at the temperature of 1000 °C and to achieve nearly complete boron activation which is demonstrated in Fig. 6.
After complete processing of deflection sensing piezoresistors and actuating heaters with PDE piezoresistors cantilever chips were mounted on chip carriers and the sensitivities were investigated at the Technical University Ilmenau by cantilever deflection measurements using a laser vibrometer produced by SIOS. To the piezoresistive bridge a voltage of $V_0 = 1$ V was supplied. The actuator voltage from 0 V to 0.5 V in steps of 0.1 V was supplied by an Agilent 33250A signal generator.
The sensitivity of the piezoresistors is defined as the change of their resistivity ΔR per unit deflection Δz and is calculated measuring the change of the bridge signal ΔV:

$$S = \frac{\Delta R}{\Delta z} = \frac{2 \cdot \Delta V \cdot R}{V_0 \cdot \Delta z} \qquad (1)$$

The PDE processing (10 nm B deposited, Si^+ irradiation, 400keV, $10^{15}cm^{-2}$) results in several kΩ piezoresistors with sensitivities of $(10\text{-}20)x10^6$ $\Omega{\cdot}m^{-1}$. The obtained averaged sensitivities of about $15x10^6$ $\Omega{\cdot}m^{-1}$ for shallow PDE processed piezoresistors can be assumed as very good. Additionally, the piezoresistors are giving very stable and reliable results. The thermal noise is very small allowing a deflection resolution of 0.1 nm. Compared to deep implanted piezoresistors (B^+, 10 keV, $5x10^{14}$ cm^{-2}, annealed at 950 °C, 30min) with a pn–junction depth of x_j = 200-250 nm and sensitivities of approx. $8x10^6$ $\Omega{\cdot}m^{-1}$ the PDE processed shallow piezoresistors show two times higher sensitivities.
The 1 keV B^+ implantation seems to be a less robust process compared to conventional implantation (e.g. at E ≥ 10 keV) and probably also compared to PDE processing using thin layer boron evaporation, 400 keV Si^+ irradiation and short time in-diffusion. For example, at low energy implantation (E ≤ 1 keV) the implantation process conditions (e.g. vacuum base pressure < 10^{-5} Pa in the implantation chamber) are very important to avoid ion neutralization and therefore broadened boron profiles. Furthermore, remaining surface layers (e.g. SiO_2) can significantly reduce the introduced boron concentration. From investigations of different kinds of USJ fabrication we can conclude that a further decreasing of the pn-junction depth of PDE processed boron profiles can be achieved by moderate doping of the n-type

substrate. This can be done by ion implantation with phosphorous (or arsenic) ions up to the concentration level of $1x10^{18}$ cm^{-3} to compensate the deeper tails of the boron profiles. The expected pn-junction depth can be than below 20 nm. The influence of the high n-type doping level on functionality and noise of the integrated piezoresistors in AFM cantilevers has to be investigated.

4. Highly boron doped heater and interconnect lines

The p^{++}-technology concerns with the fabrication of highly doped line-pattern for the cantilever deflection actuator (heater) using conventional boron ion implantation. The heater is connected through p^{++}-interconnects and through metal (Al) contact lines to the heat current source. Additionally, high doping by boron implantation is also used for the formation of p^{++}-interconnects between the cantilever deflection sensor elements (piezoresistors) and the corresponding Al metal contact lines. To achieve a minimum heat dissipation in the heater p^{++}-interconnects the sheet resistance of them must be as low as possible. On the other hand, the minimum sheet resistance of highly boron doped layers is limited by the boron solubility in silicon at a given diffusion or implantation annealing temperature. For example, at 1000 °C the maximum boron concentration in Si is $1x10^{20}$ cm^{-3} leading to a specific resistivity of 1.2 mΩ·cm and a corresponding sheet resistance of 12 Ω/square for a 1 µm thick layer. Therefore, the aim of the p^{++}-technology was the fabrication of highly boron doped layers by ion implantation for the heater element and interconnects with possibly low resistance of interconnects and with $R_{interconnect} \leq R_{heater}$. For this purpose, simulations using the CrystalTRIM and TESIM codes (simulation of as-implanted and annealed boron profiles, respectively) [11,12] for higher energy and doses were carried out.
An implantation energy of 60 keV and a dose of $4x10^{15}$ cm^{-2} followed by a 20 min furnace anneal at 1050 °C resulted in a plateau of the max. boron concentration at $5x10^{19}$ cm^{-3} which is already close to the solid solubility limit of boron in Si. The sheet resistance of the p^{++}-areas was measured as 27 Ω/square for E_1 = 30 keV and 25 Ω/square for E_2 = 60 keV (see Fig 4, red line). So the higher energy yields only a 7 % decrease of the sheet resistance. Further lowering of the sheet resistance of the p^{++}-areas can be achieved by two implantation steps at different energies (e.g. E_1 = 30 keV and E_2 = 60 keV) and at increased fluence of D = $4x10^{15}$ cm^{-2} with a post-implantation annealing in a conventional furnace for 20 min at 1050 °C.
During technology development for PRONANO cantilever arrays fabrication, simulations were carried out on SOI substrates with a device layer thickness (= cantilever thickness) of 2 µm. Fig. 6 shows a cross-section through parallel p^{++}-interconnect and piezoresistor areas after full processing.

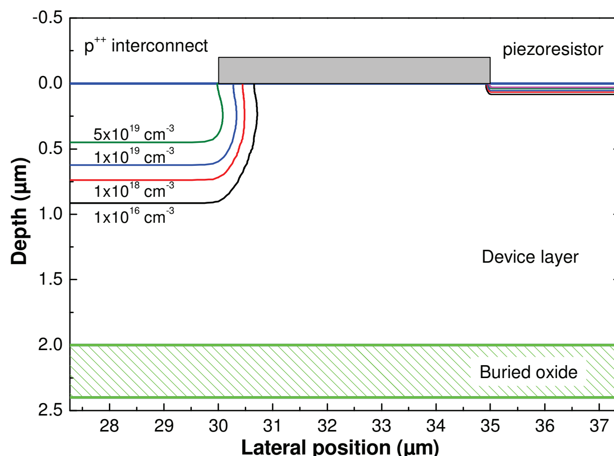

Fig. 6:
FLOOPS simulation of PRONANO cantilever processing of implantation and annealing on SOI wafer. The distance between p^{++} interconnect and the piezoresistor on the mask is 5 µm. Iso-concentration lines of the boron concentration are shown for both boron doped areas.

It can be observed that the boron from the p^{++}- interconnect line diffuses a substantial amount in lateral direction, due to the high concentration gradient in lateral direction at the mask edge and the long annealing time of 20 min at 1050 °C. In contrast, the boron from the piezoresistor area does not diffuse very far, due to shorter RTA annealing of the shallow boron implant. Overall there is still a 4 µm separation between the p-n junctions of both lines, so for moderate reverse-bias voltages (≤ 5…10 V) applied to the piezoresistor and heater a sufficient insulation can be expected. The limitation of the device layer thickness to 2 µm does not have an impact on the developed technology so far.

5. Summary

Ion implanted silicon piezoresistors as shallow pn-junctions with $x_j < 100$ nm and with appropriate sheet resistance have been fabricated and applied to highly integrated AFM sensor arrays using either low energy (1 keV) B^+ ion implantation and rapid thermal annealing or high energy (400 keV) Si^+ ion implantation (PDE) and subsequent short-time boron in-diffusion into n-type silicon.
It was shown that using the PDE process the pn-junction depth x_j can be decreased down to 20 nm and that this technique is fully compatible with silicon sensor or standard CMOS processing. It was demonstrated that the so called PDE process can be successfully applied to the fabrication of shallow piezoresistors showing increased deflection sensitivities of $(10\text{-}20)\cdot 10^6\ \Omega\cdot m^{-1}$ compared to conventional implanted ones. Recently, it was published [15] that this technique will be applied also in the ULSI technology (45 nm technology) to fulfil requirements for pn-junctions in terms of small junction depth and low sheet resistance. Additionally, the piezoresistor fabrication processes was evaluated in combination with the full AFM array fabrication process.

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