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pHEMT based power detectors for radars

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Summary:

This paper presents power detector designs using pseudomorphic High-Electron-Mobility Transistor (pHEMT) technology to address limitations inherent in conventional diode-based power detector systems. Based on commercially available CEL 3520k3 pHEMT, two detector configurations are investigated. The Angelov model establishes the non-linear relationship between drain current and voltage parameters. The designs are simulated using Keysight ADS and measured at 20 GHz. A dynamic range of 28 dB, from -30 dBm to -2 dBm for a gate voltage of -0.8 V, is measured. This extended range proves pivotal for enhancing the performance of radar systems operating at higher input powers.

Keywords: radar, power detector, pHEMT, square-law, medical radar.

Introduction

The field of radar technology is constantly evolving, with a persistent drive towards increased sensitivity, bandwidth, and improved performance. Many advances have been made in the system-level architecture and sub-system levels, including low-noise amplifiers, mixers, ADC, and signal processing [1][2]. Similarly, power detectors are a sub-system that converts incident power to a proportional output voltage for direct down-conversion in radar receivers. The overall dynamic range of the radar receiver can be affected by the linearity of the detectors.

Conventionally, diode-based power detectors are used due to their square-law characteristics, but they are limited to low input powers, without calibration or matching methods. This affects the operating range of the radars as they cannot be used for high input powers. Although correction methods can increase this operating range, it makes the signal processing chain more complex, ultimately increasing cost and complexity. The linearity of radars can be improved by utilizing the pHEMT technology. It has emerged as a promising solution, offering a commercial off-the-shelf solution for high-frequency radio receivers and radars.

This work focuses on designing and measuring commercially available pHEMT (CEL 3520k3) [3] based power detectors. Two different detector topologies are considered, and their performance is evaluated through measurements.

Detector Design

The I-V relationship of a diode has an exponential relationship. In case of pHEMT technology, the I-V relation is more complex as the current is a function of both V_{ds} (drain-source) and V_{gs} (gate-source) voltages.

$$I_{ds} = I_{pk0T} * (1 + \tanh(\psi)) * \tanh(\alpha V_{ds}) * (1 + \ \wedge \mathrm{V_{ds}}) \quad (1)$$

Eq.1. describes drain current characteristics derived from the Angelov model [4], where two hyperbolic tangent functions determine the dependence of the current on V_{ds} and V_{gs}. I_{pk0T} is a scaling factor, and the dependence on V_{gs} is determined by another function, which is contained in ψ and is given by Eq. 2.

$$\psi = P_{1m}T_1 + P_2T_1^2 + P_3T_1^3 \quad (2)$$

P_2 and P_3 are fitting parameters, and T_1 contains V_{gs} dependency as shown in Eq. 3.

$$T_1 = V_{gs} - V_{pkm} \quad (3)$$

P_{1m} is also described by a function of V_{ds}, which is a hyperbolic cosine function as shown in Eq. 4.

$$P_{1m} = P_{1T}\left(1 + \frac{B_1}{\cosh^2(B_2V_{ds})}\right) \quad (4)$$

For a more precise and complete model, to represent the saturation region, a factor ∧ is added to the current equation so that the slope in the saturation can be preserved instead of having perfectly saturated currents. Temperature dependences have not been considered as its effects should not be considerate in small signal operation.

Two different detector circuits are investigated where the incident input power is applied to the drain terminal of the transistor. In contrast, the gate terminal is fixed to a specific bias voltage. The equations for drain current can be simplified for such specific operating conditions. For a constant gate voltage, the value of T_1 can be considered constant and for small values of $V_{ds,}$ P_{1m} is approximated by the value of P_{1T}. Thus Eq. 1 reduces to a single hyperbolic tangent function controlled by varying V_{ds} as shown in Eq. 5. The term β represents the simplified $\tanh(\psi)$ function. Therefore, the above equations can be simplified for analytical understanding and analysis.

$$I_{ds} = I_{pk0T}(\beta) * \tanh(\alpha V_{ds}) * (1 + \ \wedge \mathrm{V_{ds}}) \qquad (5)$$

The output voltage is low pass filtered at the output and is dependent on the DC current and the load resistance, as the overall current is a function of the input power through Eq. (5). The low pass output voltage is also a function of the input power. From Eq. (1), (2), (4), and (6), it follows that the drain current is a non-linear function of V_{ds} and V_{gs}.

$$I_{ds} = F(V_{gs}, V_{ds}) \qquad (6)$$

In Fig. 1, detector D1, the transistor produces a DC component of the current due to switching caused by the periodic input incident power. All higher harmonics which are produced are shorted by the filter at the output. In Fig. 2., detector D2, a typical common gate topology is used. For both circuits, the output voltage is measured after a low pass filter, which is formed by R_L and C_L.

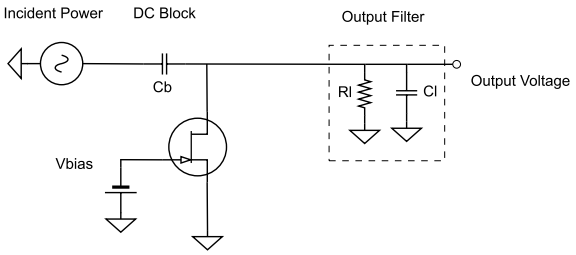

Fig. 1. Detector D1: the transistor acts as a non-linear resistor due to switching caused by the input. The output voltage is obtained after a low pass filter.

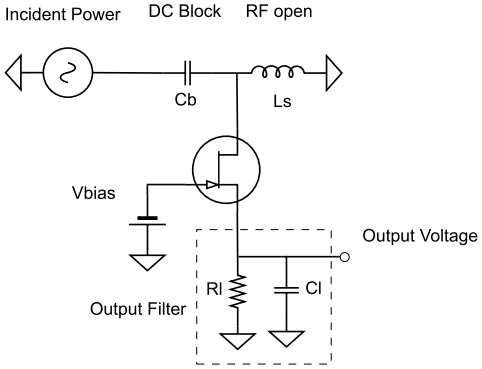

Fig. 2. Detector D2: common gate topology where the output voltage is at the source terminal of the transistor.

The design parameters and values for the components are chosen through simulation using Keysight ADS. The Modelithics library, which contains suitable models for the pHEMT and passive components, is used. This significantly reduces the design time and effort as the models already incorporate measured transistors on specific substrates and the uncertainty when the actual design is implemented.

Implementation and Measurements

The two circuits were manufactured on a Rogers 4350 substrate with a thickness of 0.254 mm. A 100 nF blocking capacitor, C_B, is used to isolate the measurement instrument and the detectors. A 100 nF capacitor, C_L, and a 10 kΩ load resistor, R_L, is used to implement the low-pass filter for both designs. The RF open inductor, L_s, in detector D2 is implemented using a quarter-wave butterfly stub. Additionally, a low pass filter is used at the gate of the transistor to bias the transistor and avoid any RF leakage. The fabricated circuits are shown in Fig. 2.

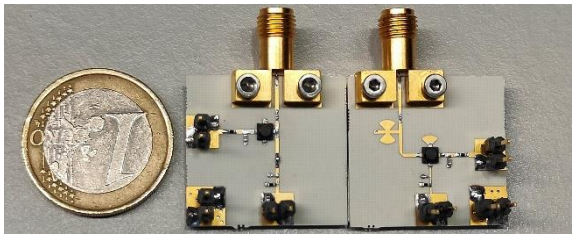

Fig. 3. The fabricated designs: detector D1 (right), detector D2 (left).

Keysight PNA-X was used to measure the S-parameters for both detectors. The input power is swept from -30 dBm to 10 dBm. The output voltage was measured using an Agilent oscilloscope.

Results

The circuits were measured at 20 GHz, for an input power from -30 dBm to 10 dBm, and two

gate voltages of -0.6 V and -0.8 V. Fig. 4. (a) and Fig. 5 (a) show the S-parameters of the two circuits and Fig. 4 (b) and Fig. 5 (b) show the output voltage in dependence of input power. Linear increase in voltage with increasing power is observed in both the designs, but the range is different for each operating condition. With a gate voltage of -0.8 V, in detector D1, the linear range extends from -30 dBm to -2 dBm, after which the output voltage shows saturation, whereas, for detector D2, the linear range is limited to -12 dBm. The linear operating range for a gate voltage of -0.6 V is relatively small in both cases, extending only to -20 dBm. The S-parameters also show similar behavior where the reflection coefficient is constant for lower input powers and gradually increases as the output voltage starts to saturate. An important point is that the S-parameters may become unreliable at high input powers as the small-signal condition does not apply.

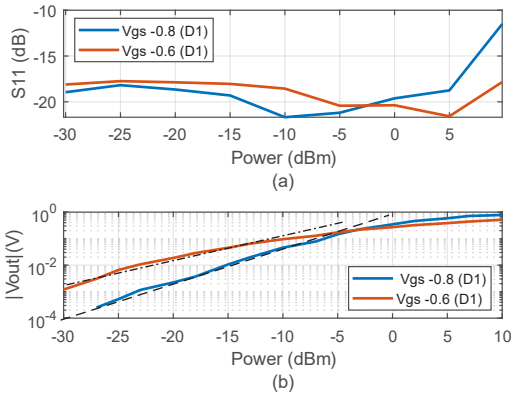

Fig. 4. Measured results detector D1: (a) S-parameter and (b) output voltage, for varying input powers.

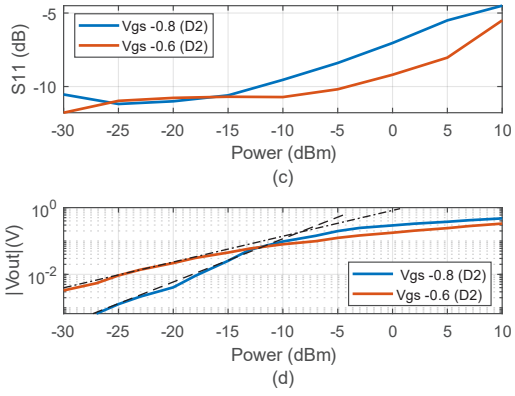

Fig. 5. Measured results detector D2: (a) S-parameter and (b) output voltage, for varying input powers.

Conclusion

Two power detector circuits were designed and fabricated for operation at 20 GHz. S- parameter and output voltage measurements were performed for input powers ranging from -30 dBm to 10 dBm, for each, two gate voltages of -0.8 V and -0.6 V. A limited dynamic range is observed for gate voltages of -0.6 V. Whereas, detector D1 provides a more extensive dynamic range of 28 dB, from -30 dBm to -2 dBm, for a gate voltage of - 0.8 V. The dynamic range increase helps maintain optimal radar system performance when higher input power is expected. This reveals the advantages of using pHEMT-based power detectors over diode-based power detectors.

References

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