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AI-supported PDN Design for PCBs in Automotive Applications

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Abstract

Due to market trends such as electronic vehicles and autonomous driving, the technological complexity of electronics for automotive applications is increasing. The rising development requirements motivate the usage of AI modules in PCB design to obtain functionally secure and reliable layouts faster. This contribution presents a prototype PCB layout tool with AI-supported features for the design of power delivery (PDN). It supports PCB developers with real-time feedback for the choice of types and positions of decoupling capacitors using Convolutional Neural Networks (CNN), suggests PDN-designs using Reinforcement Learning (RL) agents, and integrates into workflows with proprietary design tools that are common in industry-use such as ZUKEN eCADSTAR or Altium Designer.

1 Introduction

Modern motor vehicles typically feature a variety of safety-critical electronic systems such as ABS, ESC or ACC. More recently, they have increasingly included further systems and functions such as compact sensor systems with real-time sensor fusion to capture their surroundings and complex steering systems. This increases the overall system complexity and raises the demands for the design of PCB layouts in automotive applications. To manage this increasing complexity, AI modules are being incorporated into the development process to automate design steps and thereby speed up design iterations and improve efficiency and safety, which are critical on the path towards autonomous driving.

An important part of the PCB design process is power integrity (PI). PI includes a variety of design tasks related to power supply, power demand, and control of voltage and current. One aspect of PI tasks is the design of the power delivery network (PDN). The PDN guarantees the power supply of integrated components (ICs) across the entire range of operating frequencies. This involves the selection and placement of voltage regulation modules (VRMs), power management ICs (PMIC), switching regulators for lower frequencies (~1 kHz to ~5 kHz), bulk capacitors for lower to medium frequencies (up to ~1MHz), decoupling capacitors for medium to high frequencies (up to ~100 MHz) and finally the geometry and layer stack of the power and ground planes for the highest frequencies ([1]).

To validate a design against the PDN requirements of a given IC, it has to be ensured that the impedance, as seen by the IC's power pins, stays below the given bounds that are specified by the manufacturer across the range of operating frequencies. The impact of the choice of decoupling capacitors on the impedance over frequency curve depends on their capacitances, ESL values, ESR values ([2]) and positions ([3]). Besides staying below the target impedance, other objectives include the minimization of area use, part costs and manufacturing costs due to, e.g. the need for additional vias.

1.1 Previous work

Physical full-wave simulations can be performed to model the electrical processes to obtain an accurate impedance prediction for a given PDN design without expensive measurements. Such simulations are typically time-intensive, and many impedance predictions are required to generate sufficient training data for AI modules, which motivates the use of faster, numerical models. In [4], Zhang et al. present a faster calculation approach using a boundary element method and in [5], they present a CNN architecture for even faster, accurate impedance predictions. Shoaee et al. show another ANN-based fast impedance prediction in [6].

Different approaches have been presented in the literature for the automated selection of decoupling capacitor types and automated placement. In [7]-[9], genetic algorithms are used to solve PDN problems with a minimal number of decoupling capacitors. In [10] and [11], Zhang et al. present DQL- and PPO-based reinforcement learning approaches for automatic placements that can solve PDN problems with runtimes on the order of minutes to hours and compare their results to classical optimization and genetic algorithms, which are slower and provide less optimal results.

1.2 Our Contribution

This paper presents our prototype design tool, BerEDA, which utilises various AI modules to support PDN design interactively. This includes a CNN-based impedance prediction module for real-time feedback during PDN design, a colour guide for decoupling capacitor placement and an RL agent for automated decoupling capacitor selection and placement. Unlike previous approaches, we focused on fast results for interactive use and trained our RL agent for settings in which solutions can be returned within four to six seconds.

2 AI-support layout tool prototype

2.1 Layout Tool Prototype BerEDA

All AI modules presented in this paper are implemented as features of the BerEDA tool suite, which is being developed in-house to serve as a software demonstrator for various prior algorithmic contributions to PCB design automation ([12]-[15]). The tool can import and visualize designs from ZUKEN eCADSTAR, Altium Designer and its native XML format and apply various auto-placement and legalization algorithms. Algorithmic or manual changes in component positions can be exported back to commercial tools.

2.2 Real-time impedance prediction and colour guide

During the placement and movement of decoupling capacitors and ICs, a CNN-based fast impedance prediction, using a modified variation of the architecture of [5], is shown and updated in real-time (**Figure 1**).
If a target impedance curve is provided, an additional colour guide is shown when selecting a decoupling capacitor. It marks suitable placement positions that guarantee predicted impedance values below the target impedance (**Figure 2**).

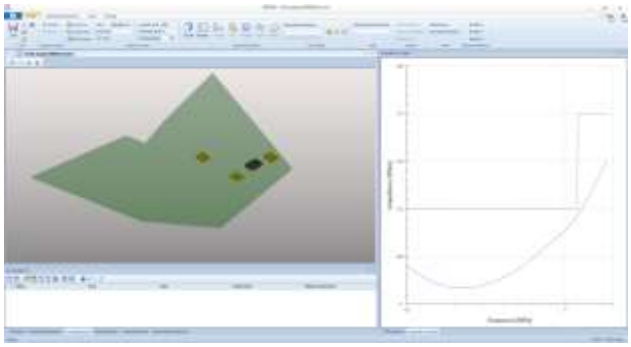

Figure 1 Real-time impedance prediction (blue curve) is shown together with target impedance (red curve) for a given PCB design with IC and various decoupling capacitors placed on the left.

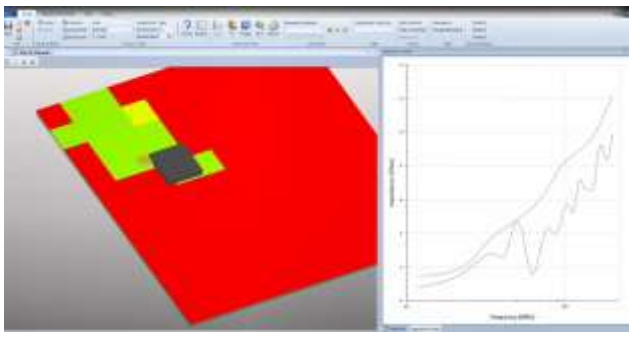

Figure 2 Real-time colour guide for suitable positions for the selected decoupling capacitor such that the predicted impedance (blue) stays below the target impedance (red).

Our CNN impedance prediction model was trained using algorithmically generated random designs labelled with impedance curves using the fast ZUKEN eCADSTAR PI Engineer. Due to the limited resolution of the discretization scheme in [5], which reduces each design to three 16×16 matrices for an up to 20×20cm² design, we also tested 32×32 discretization to support more fine placements. Our experiments yielded sufficiently close predictions to our ground truth (the ZUKEN simulator); a worst-case example is shown in (**Figure 3**).

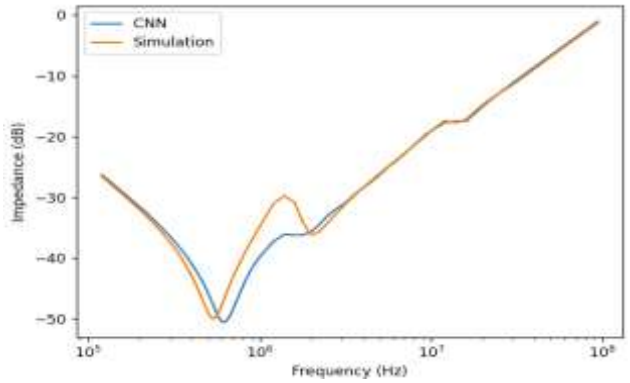

Figure 3 Worst-case impedance prediction (blue) vs simulation (orange).

The impedance prediction modules were initially implemented using TensorFlow ([16]) and PyTorch ([17]). The models were then integrated into the native C++ application BerEDA using ONNX ([18]) to avoid the overhead and latency of a Python environment in real-time impedance prediction.

2.3 RL-based Automated Decoupling Capacitor Selection and Placement

To support automated PDN design, we implemented a Reinforcement Learning algorithm into the BerEDA tool suite. Given a board shape, an IC with an impedance specification, it selects decoupling capacitor types and positions until the specification is met. Unlike in [11], emphasis is placed not on optimality but on fast results. In tests, the agent was able to solve roughly 87% of the generated test cases using DQN-learning with a CNN-based Q-network similar in structure to the architecture shown in [5]. Solutions were usually found in four to six seconds; an example of a solved test case is given in (**Figure 4**).

Figure 4 Example of design with single IC before and after RL-based automated decoupling capacitor selection and placement.

The action space was limited to selecting one out of six decoupling capacitor types and placing it on the top or bottom layer in one of 5×5 grid cells around the IC for a total of

300 possible actions. The reward function returned -100 points for an illegal placement, 10 points for a legally placed decoupling capacitor and 100 for a placement that solved the given problem with a discount factor to incentivize solutions with as few decoupling capacitors as possible. The reward converged after roughly 8000 training steps with 1000 attempted placements each (**Figure 5**).

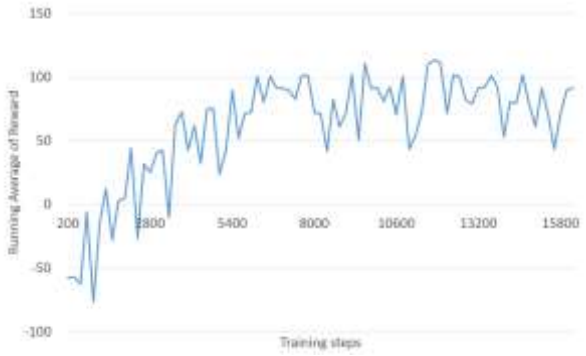

Figure 5 Convergence of RL training reward.

The OpenAI/Gym library ([19]) was used to implement the environment. The RL agents were then implemented using tf-agents ([20]).

2.4 Integration into Commercial Workflows

To make our AI modules available to developers using commercial design tools, interfaces were implemented to ZUKEN eCADSTAR and Altium Designer.

In the case of ZUKEN eCADSTAR, a parser has been written to import proprietary ZUKEN RIF files as designs into BerEDA. For the other direction, changed component positions can be written back using a CSV format.

For Altium Designer, an add-on was implemented using the Altium Developer SDK to export design information into the native BerEDA XML format (**Figure 6**) and to import component positions that were changed after applications of auto-placement algorithms in BerEDA.

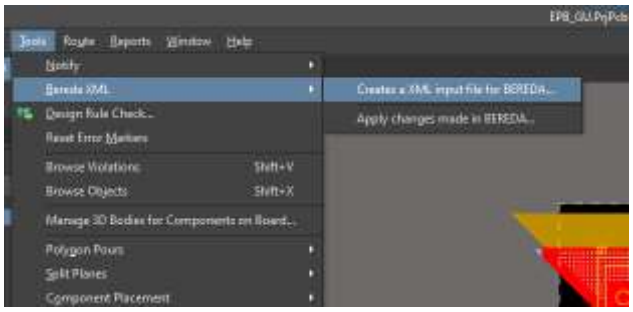

Figure 6 Integration of BerEDA Export/Import-plugin into Altium Designer.

3 Conclusion

In this contribution, we have demonstrated the implementation and use of AI modules for PDN design in a layout tool prototype that can be incorporated in industry-grade PCB design workflows by interfacing with commercial tool chains. The presented AI modules were adapted for interactive use, which requires particularly fast results. They provide capabilities for real-time impedance prediction, placement guides and selection and placement suggestions for decoupling capacitors.

4 Acknowledgements

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