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Total-Ionizing-Dose Radiation Hardness of Inter-Layer Dielectrics in a 130 nm SiGe BiCMOS Technology

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Summary: This paper investigates the influence of interlayer dielectric layer (ILD) oxide stacks on the underlying silicon bulk. MOS-like test structures with ILD stacks composed of CVD Si oxides and differently processed SiN layers were used for measurements of transistor characteristics and gated-diode measurements before and after irradiation with 10 keV x-rays. Strong influence of the detailed processing conditions of the silicon nitride layers on the Si substrate was found. Total ionizing dose irradiation response of the ILD stacks was very similar.

Keywords: Radiation hardness,x-ray, TID, JFET, CMOS

Introduction

Total ionizing dose (TID) effects due to ionizing radiation are an essential concern in radiative environments. TID causes degradation of MOS transistor parameters such as drain leakage current and threshold voltage due to charge trapping in oxides and interface trap generation at oxide-silicon interfaces. For devices with lateral drift zones like LDMOS transistors [1] charges generated in ILD oxides/nitrides might become relevant. We report on the TID behavior of a SiN/SiO stack directly on top of the Si active area irradiated with 10 keV x-rays. The influence of processing conditions of a 50 nm silicon nitride contact stop layer were investigated using a MOS test structure with the ILD stack as gate oxide and the first metallization layer as gate (ILD-MOS). In addition to the standard MOS characteristics, the test structures allow for measurements in the 'gated-diode' configuration.

Experimental

Test Structures

ILD-MOS preparation was carried out using IHPs 130 nm SiGe BiCMOS Technology starting with a 10 nm TEOS SiO_2 layer on the p-type Si substrate. The M1 metal layer is used as gate. An overview of the oxide stack is given in Table 1.

Two variants of the ILD-MOS with different PECVD SiN contact stop layers (SiN type I and type II) were used. Compared to SiN type I, SiN type II deposition uses higher RF-power and a larger NH_3 to SiH_4 gas flow ratio. SiH_4 gas flow and deposition temperature are identical for both films. SiN film properties vary according to changes in the gas flow ratios and plasma power. In particular, by changing the deposition parameters, composition and stress of the films can be changed. A schematic cross-section of the ILD-MOS is shown in Figure 1. ILD-MOS width and length are 1300 µm and 75 µm, respectively. Multiple devices are connected in parallel. Total gate area is 2×10^{-3} cm^2.

Tab. 1: Layer thickness of the stack

Layer	Thickness in nm
M1	420
CVD oxide	510
Contact Stop Nitride	50
Silicide Blocker Nitride	70
TEOS Silicon Oxide	10
p-substrate	–

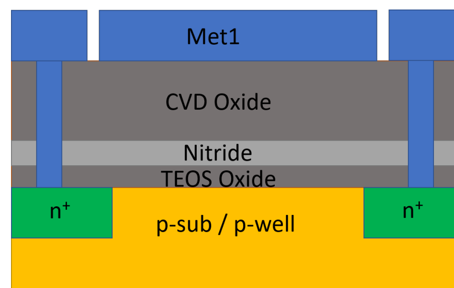

Fig. 1: Schematic cross-section of ILD-MOS.

Measurement Set-Up

Irradiation was carried out with 10 keV x-rays with a dose rate of 1.5 krad(Si) min^{-1} in a Precision iR160 x-ray irradiator equipped with a manual probe station. The irradiation dose is varied stepwise with a maximum dose of 200 krad(Si). During irradiation the gate was biased at 20 V with all other contacts grounded.

In situ on-wafer electrical characterization was carried out using a Keithley 4200 semiconductor parameter analyzer.

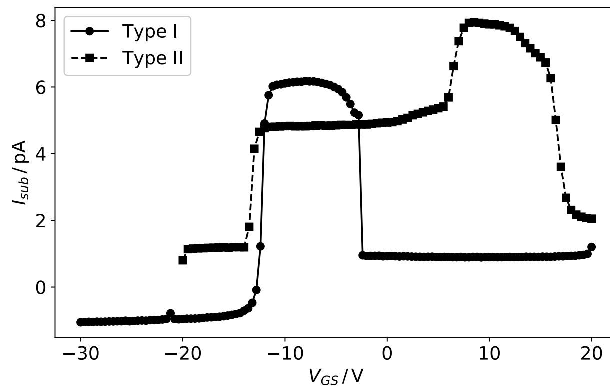

Fig. 2: Gated-diode substrate current I_{sub} vs. gate voltage V_{GS} for Type I and Type II ILD-MOS devices.

In addition to the measurement of standard MOS device characteristics, gated diode measurements [2] were carried out. The gated diode technique allows for calculation of the interface trap density D_{it} by measuring the gate voltage dependence of the substrate current. A gated-diode measurement involves keeping the diode at a constant reverse voltage and measuring the change in substrate current when the gate is swept from accumulation towards inversion. In accumulation only the n$^+$(Drain/Source) / p-sub diode leakage current is obtained. At flatband voltage V_{FB}, where the gate region becomes depleted, a strong increase in current is observed (see Figure 2). This is due to the minority carriers generated in the Si bulk under the gate and at the gate-substrate interface, which are then swept towards the substrate contact. The substrate current I_{sub} in this region is a measure for the interface trap density D_{it} and the volume minority carrier generation. At the point where inversion is reached, the current drops due to the screening of interface traps by the inversion layer and only volume carrier generation is active. In our measurements the n$^+$(Drain/Source) / p-sub diode is reverse biased at 5 V.

Results and Discussion

Pre-irradiation Measurements

A histogram of the ILD-MOS threshold voltages V_{th} is shown in Figure 3. For ILD-MOS type I a relatively narrow V_{th} distribution around −13 V is found. This implies formation of an inversion layer underneath the ILD stack even without any externally applied gate bias.

The threshold voltages for ILD-MOS type II devices are positive but display a broad distribution ranging from 2 V to 18 V. A detailed inspection of the measurement data shows that the highest V_{th} values are found in the wafer center. This hints to a strong dependence of the SiN type II film properties on the detailed processing conditions. Defects in silicon nitrides can act as charge trapping centers and silicon nitride layers exhibit charge storage characteristics for both electrons and holes. We ascribe the negative threshold voltages for type I ILD-MOS to fixed positive charges in the SiN films generated during the PE - CVD deposition and / or subsequent processing steps.

The increased NH_3 to SiH_4 gas flow ratio during SiN type II deposition leads to larger N and H content. Hydrogen in the type II layers can initially passivate dangling bonds and charge traps resulting in less fixed charge after deposition compared to type I films.

The contact stop nitride also influences the properties of the underlying oxide-Si substrate interface as demonstrated by the ILD-MOS subthreshold slope in Figure 4 and the gated-diode measurements shown in Figure 2 and Figure 5. The gated-diode characteristics of type I and type II SiN films in Figure 2 show pronounced differences. Flatband voltage V_{FB} is more or less equal. In contrast, the onset of inversion for the type II device is found at positive voltages. This corresponds to the positive threshold voltages of type II devices in Figure 3. The origin of the step in the measured substrate current observed for type II devices is currently not clear.

As shown in Figure 5 using the maximum gated-diode substrate current as a measure of interface trap density D_{it}, for ILD-MOS type II a larger interface trap density is found compared to type I devices. Correspondingly, the subthreshold slope SS for type I devices in Figure 3 is in general smaller than for type II ILD-MOS.

In accordance with the results for V_{th} above, SiN type II devices also show larger variation of D_{it}. The root cause for the different interface trap densities at the ILD - Si-bulk interface for type I and type II SiN contact stop layers is difficult to pin down. The different SiN films can exert different amounts of stress on the oxide - Si substrate interface and induce different interface trap densities. Additionally, different rates of H outdiffusion from the SiN films can lead to different amounts of interface trap passivation at the interface.

Despite the marked differences observed in Figure 2 and Figure 5 the overall influence of the SiN contact stop layers on the Si interface is small. Note that most Si interface traps are passivated after processing, leading to small interface trap densities in the 10^9 cm^{-2} to 10^{10} cm^{-2} range. Irradiation leads to interface trap generation by depassivation of dangling bonds at the interface and the post-irradiation results presented below show, that both ILD stacks behave very similar under irradiation with a strong increase in D_{it}, which completely overwhelms any differences observed in the as-processed films.

Post-irradiation measurements

Measurements after increasing irradiation doses for typical type I and type II devices are shown in Figure 6. Total ionizing dose response of a MOS system is due electron/hole creation in the

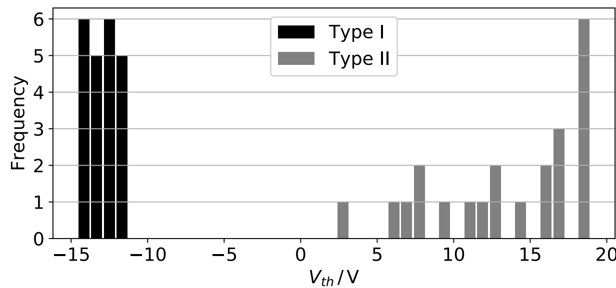

Fig. 3: Histogram of ILD-MOS threshold voltages V_{th} extracted from drain-source current I_{DS} vs. V_{GS} gate-source voltage ILD-MOS transfer characteristics.

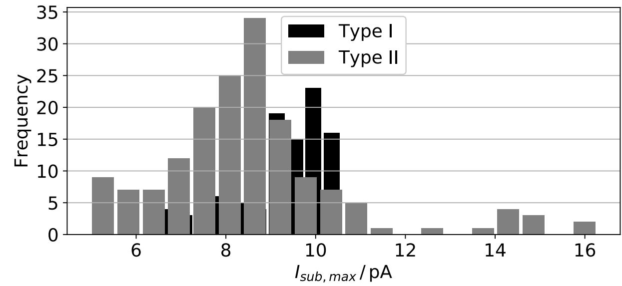

Fig. 5: Histogram of gated-diode substrate current I_{sub} vs. gate voltage V_{GS} for Type I and Type II ILD-MOS devices.

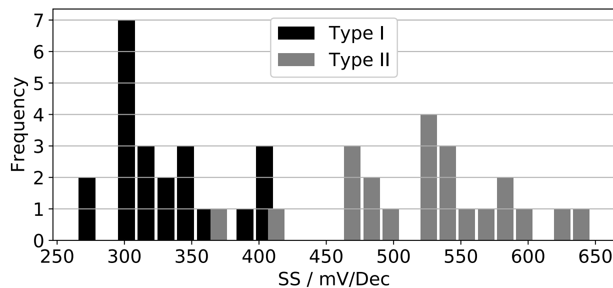

Fig. 4: Histogram of ILD-MOS transfer characteristics sub–threshold slopes SS.

surrounding oxides [3]. In oxides, electrons are generally much more mobile than the holes and are swept out of the oxide under the influence a applied voltage. The holes remain in the oxide and cause a negative threshold voltage / flatband voltage shift. With increasing irradiation dose the ILD-MOS threshold voltage in Figure 6 a) and b) shifts to more negative values indicating the generation of radiation induced positive charges in the ILD oxides.

For the highest doses in Figure 6 a) and b) an increase of the sub-threshold slope is discernible in the ILD-MOS transfer characteristics. The ILD-MOS sub-threshold slope increase indicates the generation of interface traps. It is well known, that in addition to the generation of fixed oxide charges, irradiation of a MOS system leads to buildup of interface traps at the Si/Oxide interface.

This observation is corroborated by the gated diode measurements in Figure 6 c) and d), where a strong increase of the interface generation current with increasing irradiation dose is found. Because of the shift of the flatband voltage by the generated positive oxide charge the substrate current peak moves to more negative gate voltages. Note that the post-irradiation curves in the figures are shifted relative to each other on the I_{sub}-axis and the pre-irradiation current values (dashed lines) are multiplied by a factor of 25. The peak form of the substrate current signal after irradiation is very similar for type I and type II devices pointing to only very limited differences in the influence of the type SiN contact stop layer type on the ILD-Si interface.

The change of threshold voltage V_{th} and flatband voltage V_{FB} as a function of irradiation dose extracted from measurements as in Figure 6 is shown in Figure 7. Saturation has not been reached and is expected for higher dose levels. A behavior of the flatband voltage V_{FB} similar to Figure 7 was observed previously in [4] after irradiation of silicon-MOS gated diode structures with high energy electron beams.

The type II device shows a stronger variation of V_{th} and V_{FB} with dose. This could be explained by a larger density of H-saturated dangling bonds in type II SiN films as described above. During irradiation the dangling bonds can be depassivated by holes generated in the ILD layers. In view of the strong variability of type II devices, it is difficult to draw general conclusions regarding the relative susceptibility with respect to ionizing radiation damage for the investigated SiN films from these results.

As expected there is very small difference in the influence of the remote SiN contact stop layers on the behavior of the Si/ILD interface under irradiation. As shown in Figure 8, ILD-MOS with SiN type I and type II SiN films show a very similar, nearly linear dependence of the interface trap density build-up under irradiation. Further investigations are planned which will explore the influence of the TEOS oxide properties on the ILD-oxide interface.

Conclusions

The construction and/or processing details of the ILD stack has a profound influence on the behaviour of the Si bulk. Even process variations in layers remote from the Si-ILD interface can modify properties like inversion or depletion at the Si surface and modify interface properties like the interface trap density D_{it}. TID response is dominated by the overall ILD oxide properties. Changes in the radiation response of the relatively thin SiN contact stop layers processing variations of the have only a minor influence.

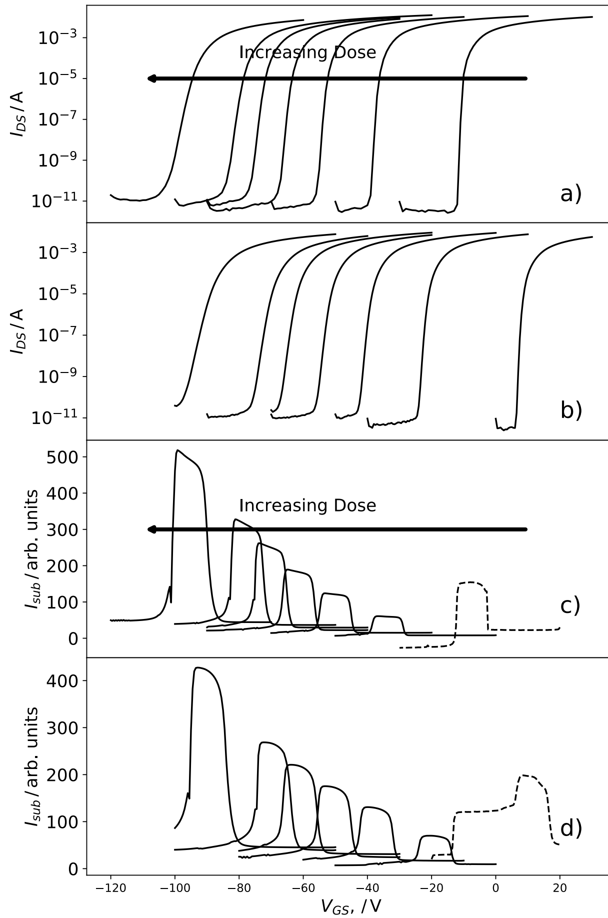

Fig. 6: a) Transfer characteristics of ILD-MOS tpye I and b) of ILD-MOS tpye II with $V_{\mathrm{DS}} = 3.3\,\mathrm{V}$ for increasing irradiation dose. Corresponding gated-diode substrate current measurements are shown in c) and d) for ILD-MOS tpye I and II, respectively.

Author Contribution

J.S. and F.K. were responsible for experiments and analysis of the results. R.S. was responsible for preparation of the ILD-MOS devices.

Competing Interests

No competing interests are present.

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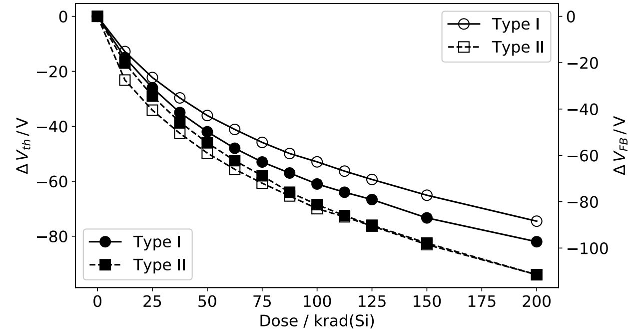

Fig. 7: Change of ILD-MOS threshold voltage ΔV_{th} (left) and ILD-MOS flatband voltage ΔV_{FB} (right) vs. irradiation dose.

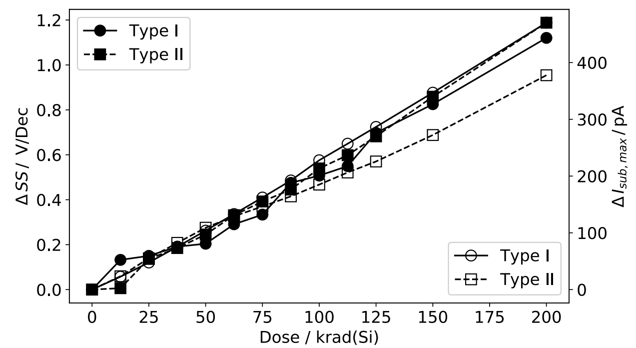

Fig. 8: Change of ILD-MOS subthreshold slope $\Delta\mathrm{SS}$ (left) ans maximum gated-diode substrate current $I_{\mathrm{sub,max}}$ (right) vs. irradiation dose

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