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Laser-based method for the fabrication of monolithically and vertically integrated MEMS sensors

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Abstract

An obstacle to further miniaturization and higher precision of MEMS sensors is the separate design of the sensor and the integrated chip. Parasitic capacitances in the bonding wires can affect the signal quality negatively. Integrating the sensor directly onto the ASIC not only eliminates this source of error, but also reduces the space requirement. One challenge to be addressed is the thermal load of the ASIC, which must not be exceeded. A solution to this problem is a two-step process. First, doped silicon for the sensor structures is deposited in an amorphous phase using PECVD. Subsequently, laser radiation is used to crystallize the silicon and achieve a conductive layer. After etching, the mechanical anchor points double as the electrical contacts of the sensor structures. Complete crystallization of this layer is therefore crucial for the functionality of the sensor. In this context, strategies for laser annealing an amorphous silicon layer over the full depth are developed, and the complete solid-phase crystallization of a 10 µm thick amorphous silicon layer is demonstrated. Furthermore, a trade-off between the full depth crystallization of the silicon layer and the functional integrity of the ASIC is identified. This tradeoff must be experimentally verified and, if proven, circumvented through appropriate processing strategies.

Keywords: MEMS, Laser annealing, Sensors, Finite Element Method, Thin Films

I. Introduction

Micro-electromechanical systems (MEMS) are popular in the sensor industry due to their versatility and robustness. In the form of inertial sensors, pressure and temperature sensors, and many other functions, they are widely used in everyday life and, despite current market fluctuations, industry growth is expected. [1] In the field of high-precision inertial sensors, a growth of $570 million is expected by 2027, with MEMS being attributed competitive potential if performance and price can be adjusted to other systems such as fiber optic gyroscopes [2].

One obstacle on the path to further miniaturization and precision of MEMS sensors is the separate design of the MEMS unit and the application specific integrated circuit (ASIC) used for signal evaluation. This architecture not only occupies a larger area, but also disrupts the sensor signals through parasitic capacitances and thermal drift in the bonding wires. [3].

Vertical monolithic integration, where the MEMS element is directly fabricated on the IC through layer deposition and post-processing, offers the potential to reduce the required space and increase the sensor precision. In this setup, the electrical interconnect of the sensor structures is provided by the mechanical anchor points.

As the thermal load of the epitaxial growth of silicon for the MEMS layer on the IC (up to 1000 °C) exceeds the destruction threshold for the ASIC (400 – 450 °C for interaction times of about 6 hours [4]), the manufacturing of the MEMS element in this way is not possible. In an alternative process, doped silicon is deposited in an amorphous phase via plasma-enhanced chemical vapor deposition (PECVD) which is possible at IC-compatible temperatures < 450 °C.

The amorphous phase results in a sheet resistance that is several orders of magnitude too high for the usage as conductive interconnect or e.g., measuring the capacitance when working with a capacitive inertial sensor. Through a thermal post-treatment, it can be transformed into a polycrystalline phase, resulting in technically relevant sheet resistances. A conventional oven process requires temperatures of > 600 °C [5], the maximum thermal load of the ASIC is exceeded as a result. In an alternative process, the amorphous silicon layer can be heated locally using laser radiation. The full two-step process is illustrated in Fig. 1.

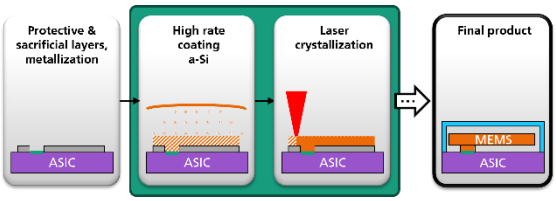

Fig. 1: Diagram of the sensor manufacturing process described in this paper. The starting point is an ASIC prepared with protective and sacrificial layers as well as a metallization layer. After etching and encapsulation the final product shows a MEMS sensor directly built onto an ASIC.

The duration of the laser process is a few milliseconds [6]. By introducing localized heat with a short process duration, the thermal load on the IC is reduced. Furthermore, literature suggests higher stress limits of the IC with shorter interaction times [4, 7]. This laser process is described here.

II. Laser-induced crystallization of silicon

The amorphous phase of silicon is a metastable state. As a result, it can be crystallized either through a melting process followed by solidification (Liquid Phase Crystallization - LPC) or through the path of solid-phase crystallization (SPC). If the starting material is doped with a dopant, the dopant atoms are incorporated into the silicon crystal lattice during the crystallization process. Optically, both the amorphous phase and the crystalline phase, as well as the SPC layer and the LPC layer, can be visually distinguished from each other in terms of color, the reason is likely a difference in the crystallite size. This is depicted in the cross section in Fig. 2. [8]

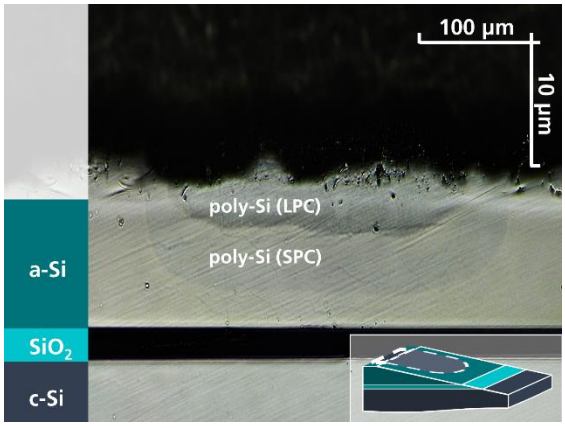

Fig. 2: Cross-section of a wafer with a substrate of single-crystal silicon (c-Si), a thermally and electrically insulating oxide layer (SiO_2), and a layer of amorphous silicon (a-Si). In the a-Si layer, areas of polycrystalline silicon (poly-Si) generated by laser irradiation are visible. A visual difference in color between SPC and LPC can be observed.

In the case of LPC, convection processes in the liquid phase are also stimulated. Material redistributions caused by this can be identified on the wafer surface under a microscope, as shown in Fig. 3. The resulting roughness should be avoided and therefore the LPC process is avoided in total.

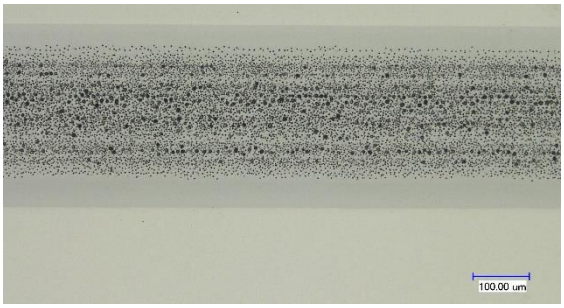

Fig. 3: a-Si surface with a trail of poly-Si. The LPC poly-Si area can be identified by the surface inhomogeneities.

The temperature range of the SPC is time-dependent. During the process described in this paper, the interaction time of the laser radiation with the material is approximately 1 - 10 ms. As a result, an SPC temperature window of approximately 980 – 1120 °C can be reached. [8]
During the laser process, three target parameters must be met to create a suitable layer for a MEMS sensor: The layer must be crystallized over the full depth. The layer must be free of cracks and blisters. The thermal load of the process must preserve the ASIC integrity. To fully crystallize the a-Si layer, a flat temperature gradient must be present in this layer, over the full thickness of the layer the maximum should be $\Delta T \leq 140\,°C$. At the same time, a temperature gradient of $\Delta T \geq 530\,°C$ must be achieved over the thermally insulating oxide layer (SiO_2) to preserve the IC compatibility of the process.

III. Methods

To evaluate the depth of crystallization, it is sufficient to examine the thickness of the differently colored layers in a cross-section. The cross-section is grinded at an angle of approximately 20° to the plane (see Fig. 1, Inlay). Since this leads to a distorted representation of the layer thicknesses, the ratio of the actual

thickness of the SiO_2 layer to the measured thickness is used as a scaling factor.
To determine the temperature distribution within the sample during the process, thermal simulations are performed. The Finite Element Method (FEM) is used for this purpose. The simulation program used is developed by Annika Völl and Thomas Bussek at the Chair of Technology of Optical Systems (TOS) at RWTH Aachen University. The program allows to simulate the heat input through laser radiation using an intensity profile and volumetric absorption. The volume elements are rectangular and equally sized within a simulated layer. Multiple layers can be modeled with their own material-specific parameters. A temperature-dependent, reversible phase transition can be modeled. [9]
The program allows the simulation of heat conduction. Convection and thermal radiation are not considered. In a comparative simulation using the COMSOL Multiphysics simulation program by Comsol Multiphysics GmbH (Göttingen, Germany), it becomes apparent that the influence of these heat transport mechanisms is negligible.
The boundary conditions are chosen according to [10] and are displayed in Fig. 4. A thermal symmetry is assumed orthogonal to the direction of motion of the laser spot.

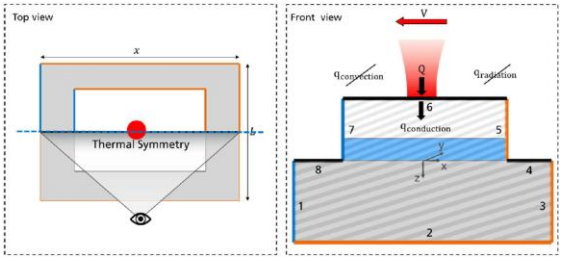

Fig. 4: Scheme of the boundary conditions used for the simulation, picture taken from [10]. Blue areas: Dirichlet boundary condition, surface is at preheating temperature. Black areas: Neumann boundary condition, heat flux q = 0. Orange areas: Insulated boundary condition: No temperature flux is possible, can only be heated by interaction with laser radiation.

As the phase transition can only be represented reversibly (e.g., a melting process), cooling processes after the end of the irradiation duration cannot be represented, as the material properties of the polycrystalline phase are again used instead of those of the amorphous phase. However, for the crystallization process itself, only the temperature distribution during the irradiation is relevant. Since the laser spot is moved over the surface, a thermal equilibrium is formed after a finite time. The simulation is evaluated only at the equilibrium point in time.
The material properties are chosen analogous to [8, 11].

IV. Sample processing

The wafers used are provided by the Fraunhofer Institute for Silicon Technology ISIT. The layer structure is listed in Tab. 1.

Tab. 1: Layer structure and layer thicknesses of the wafers used.

Layer	Thickness [µm]
a-Si	10.4
SiO2	2.45
c-Si	725

A laser system with a wavelength of 1070 nm is used. The laser radiation is directed into a galvanometric scanner with an F-theta lens attached. This enables a movement of the laser spot over the surface. Optional preheating can be done with a heating plate A sketch of the experimental setup is depicted in Fig. 5.

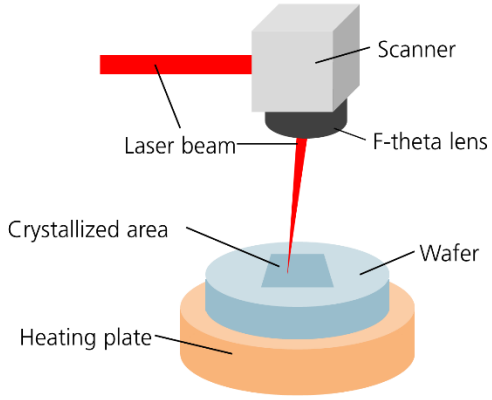

Fig. 5: Setup for the laser annealing process

With the absorption of the laser radiation, a temperature gradient is created during the annealing process (also see Fig. 6), which decreases from the sample surface to the substrate. To achieve a flat gradient in the amorphous layer, as mentioned in Chapter II, the material needs to be preheated from below. The laser-induced temperature gradient is superimposed with a counter-gradient of the preheating.
An upper limit for the preheating temperature is given by the destruction threshold of the IC. Cross-sections can be used to observe that the crystallization front follows the intensity profile of the laser beam [8]. In thermal simulations as well, the temperature profile is observed to be

almost a stamp impression of the intensity profile, see Fig. 6, left. To obtain a homogeneous crystallization depth, a so-called Tophat is used for the beam geometry, which means a constant intensity across the beam diameter, an example of which is shown in Fig. 6, right.

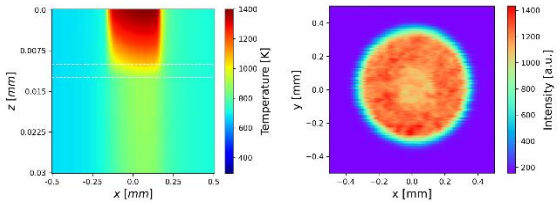

Fig. 6: Left: Cross-section of a simulated temperature profile during laser annealing, using a Tophat beam geometry. Right: Measurement of the intensity distribution of a Tophat beam geometry, measured with the beam analysis device FocusMonitor by PRIMES GmbH (Pfungstadt, Germany).

During the annealing process, the surface is scanned by the laser spot in a meandering pattern with a fixed laser scanning speed. For the selection of the laser power, fields are processed with incrementally increasing laser power. Afterwards, the power level is chosen, which's next higher level shows signs of melting on the surface. Thus, the upper temperature limit of the SPC is always reached at the surface.

V. Strategies for SPC through-crystallization

Since the upper SPC temperature limit also sets a limit on the usable laser radiation intensity, an increase in the depth of crystallization can not only be achieved by increasing the laser power. Other parameters to be varied can be the laser wavelength, laser beam geometry, interaction time or the geometry of the meandering pattern. [8]

In the experiments, the wavelength of the laser and the scanning speed of the laser spot are kept constant. The laser power is chosen, as described in Chapter IV, in a way that the upper SPC temperature limit is reached at the surface of the sample.

As observed in [8] for laser beam diameters of 330 µm and 570 µm, increasing the laser beam diameter leads to an increase in the depth of crystallization. The laser beam diameter can be increased by using an F-Theta lens with a higher focal length. This is illustrated in Fig. 7 for a larger parameter range. In this way, with preheating temperatures of 450 °C, complete crystallization of the a-Si layer can be achieved starting from a beam diameter of 570 µm, and with preheating temperatures of 400 °C, starting from a beam diameter of 850 µm.

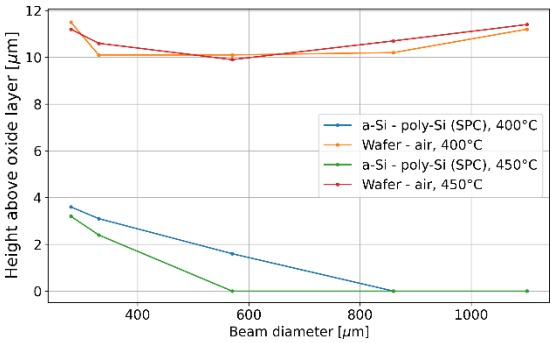

Fig. 7: Height of the interfaces wafer-air and a-Si to poly-Si above the oxide layer in dependence on the laser beam diameter. A height of 0 µm of the latter one of the resembles a through-crystallization, as achieved for the preheating temperatures 400 °C and 450 °C.

The simulation of the process with the corresponding beam diameters shows that a larger heat-affected zone leads to heat accumulation in the a-Si layer, resulting in a flatter temperature gradient. The depth of crystallization is increased that way.

However, the overlap of adjacent tracks within the scanned meander pattern has only a minor effect on the depth of crystallization. As shown in Fig. 8, the difference between a track spacing of 10 µm (~3 % of the beam diameter) and 150 µm (~45 % of the beam diameter) is only 1 µm in terms of crystallization depth.

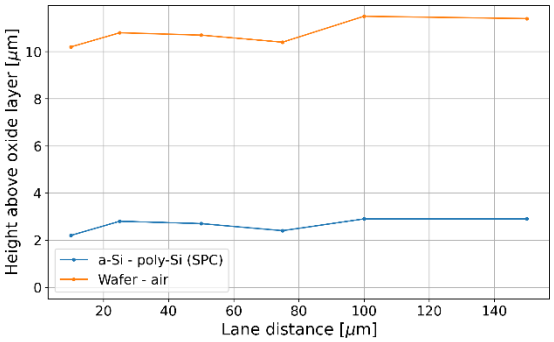

Fig. 8: Height of the interfaces wafer-air and a-Si to poly-Si above the oxide layer in dependence on the lane distance of the meander pattern. This variation is performed for a beam diameter of 330 µm with constant power and a preheating temperature of 400 °C.

During the crystallization of the a-Si layer, the interface with the oxide layer is heated to at least the lower SPC temperature limit, 980 °C. The temperature must then drop to an IC-compatible value of 450 °C across the oxide layer. This is not achieved for the given oxide layer thickness of 2.45 µm, as shown in Fig. 8 above. However, the simulation demonstrates that a thicker oxide layer not only allows for a greater temperature drop towards the ASIC but also creates heat accumulation in the a-Si layer, resulting in a greater depth of crystallization. This is illustrated in Fig. 9 below.

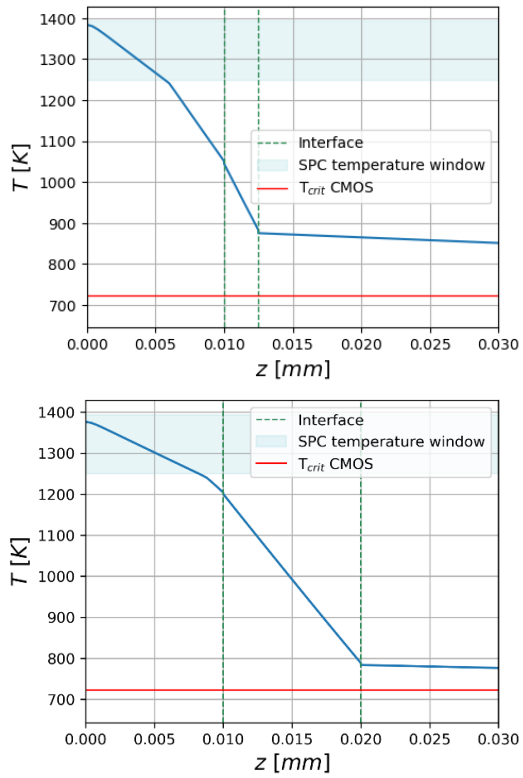

Fig. 9: Simulated temperature curves along x=y=0 in z-direction (beam width: 330 µm, preheating temperature 400 °C, 0mm being the surface). Laser power is chosen to achieve the maximum SPC temperature on the surface.
Top: 2.5 µm oxide layer thickness. Bottom: 10 µm oxide layer thickness.

Even in the shown case of an oxide layer thickness of 10 µm it can't be avoided that the temperature of the ASIC is above its destruction threshold.

Conclusion

The laser crystallization of amorphous silicon is a process step in an approach for vertical and monolithic integration of MEMS sensor and ASIC. Initially, doped amorphous silicon is deposited on the ASIC using PECVD. Subsequently, the amorphous silicon layer is heated using laser radiation and thus thermally transformed into a polycrystalline phase. To avoid surface defects, this is done through solid-phase crystallization.
The main challenge is to fully crystallize the existing amorphous silicon layer in depth while staying within the temperature window of solid-phase crystallization. Furthermore, the thermal load of the ASIC must not be exceeded.
As strategies to increase the depth of crystallization, methods for creating heat accumulation in the a-Si layer are identified. Experimental evidence shows the complete crystallization of a 10 µm thick a-Si layer. The ASIC can be protected from higher temperatures by using thicker oxide isolation layers adjacent to the a-Si layer. However, in both strategies, the thermal load of the ASIC is still exceeded. One solution to this problem would be to integrate additional insulating oxide layers, such as aluminum oxide.
Since an ASIC also contains several insulating oxide layers and it is experimentally impossible to verify if the simulated temperature distribution matches reality, further investigations into the destruction threshold of the ASIC in the laser crystallization process are pursued. For this purpose, a Daisy Chain structure on the wafer could be considered as a cost-effective alternative to using a real CMOS.

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