

Design Rules for CMOS-Compatible OECTs: Impact of Geometry and Architecture on Ionic–Electronic Transport

Nikolay Mukhin¹, Gitti L. Frey², Vadim Issakov¹, Liubov Bakhchova¹

¹ *Institute for CMOS Design, Technical University of Braunschweig, 38106 Braunschweig, Germany*

² *The Science and Engineering of Organic Electronics Research Group, Department of Materials Science and Engineering, Technion – Israel Institute of Technology, Haifa 3200003, Israel*
nikolay.mukhin@tu-braunschweig.de, gitti@technion.ac.il, liubov.bakhchova@tu-braunschweig.de

Summary:

Organic electrochemical transistors (OECTs) are promising for biosensing, but their CMOS integration is limited by insufficient understanding of geometry-dependent transport. Here, we show that OECT behavior deviates from simple scaling due to non-uniform electrochemical doping. Using physics-based finite element modeling calibrated with experiments, we analyze short-channel planar and vertical accumulation-mode OECTs. Device architecture controls electric-field distribution and active channel volume, leading to deviations from the Bernards–Malliaras model. These results establish design rules for CMOS-compatible OECTs.

Keywords: organic electrochemical transistors (OECTs), organic mixed ionic–electronic conductors (OMIECs), device performance, geometry and architecture, CMOS compatibility

Motivation and Objectives

Organic electrochemical transistors (OECTs) are promising for biosensing due to their low-voltage operation, high transconductance (g_m), and compatibility with biochemical and flexible platforms [1]. For practical sensing systems, OECTs must be integrated with compact readout and control electronics, making CMOS-compatible operation essential. Although OECTs based on PEDOT derivatives are widely studied, recent advances in accumulation-mode OMIECs are driving a shift toward alternative materials [2,3]. Thus, accumulation-mode behavior is a key requirement, as CMOS circuits rely on normally-off transistors with low static power consumption. Accumulation-mode OECTs therefore provide a more suitable basis for complementary integration than depletion-mode devices due to their off-state operation at zero gate bias and reduced standby losses [3]. Moreover, ambipolar OMIECs [4] are of special interest as they offer additional potential for CMOS integration.

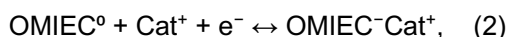
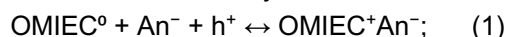
However, despite rapid materials progress, predictive modeling of accumulation-mode OECTs remains limited, particularly in understanding how geometry and architecture govern ionic transport, volumetric doping, switching dynamics, and performance trade-offs.

In this work, we address this gap by systematically investigating the influence of device geometry and architecture on the electrochemical and electronic performance of accumulation-mode n- and p-type OMIEC-based OECTs using physics-

based finite element modeling (FEM) in COMSOL Multiphysics, informed by experimental data, to derive design-relevant trends for CMOS-compatible architectures.

Methodology

We employ a physics-based FEM in COMSOL Multiphysics to simulate coupled ionic–electronic transport in accumulation-mode OMIEC-based OECTs. The model self-consistently solves the Poisson–Nernst–Planck equations for ion transport and drift–diffusion equations for electronic carriers, capturing volumetric electrochemical doping within the channel. Device parameters are calibrated using experimental data to ensure physically meaningful material and transport properties. A parametric study is performed across planar, coplanar, and vertical device geometries to evaluate the impact of architecture on key performance metrics, including transconductance, switching behavior, and ionic charging dynamics. Electrochemical doping in the model is described by:



for p- and n-type OMIECs, respectively. Here, OMIEC^0 denotes the neutral material, h^+ and e^- are hole and electron carriers, and An^- and Cat^+ represent electrolyte anions and cations. These reactions couple ionic uptake to electronic carrier density and govern channel conductivity.

Results and Discussion

To elucidate structure–property relationships in OMIEC-based OECTs, we compare planar (Fig. 1a) and vertical (Fig. 1b) architectures, focusing on how device geometry governs electric-field distribution, mixed ionic–electronic transport, and volumetric doping dynamics.

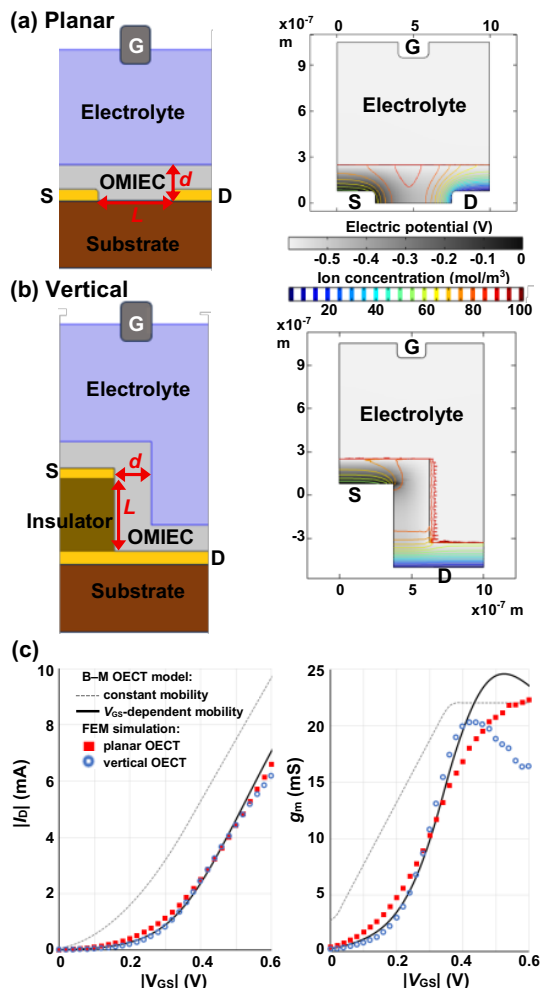


Fig. 1. (a,b) Schematic and simulated spatial distributions of electrostatic potential and anion concentration for planar (a) and vertical (b) OECTs with the same channel length (L) and height (d). (c) Transfer characteristics of a p(g2T-TT)-based OECT at $V_{DS} = -0.4$ V. The standard Bernards–Malliaras (B–M) model with constant mobility (grey dashed) and the modified B–M by gate voltage V_{GS} -dependent mobility (black) deviate from FEM simulations (colored dots).

Widely used Bernards–Malliaras (B–M) model [5] exhibits uniform channel penetration and geometric scaling, suggesting that planar and vertical OECTs can be described by the same simplified approximation form. However, in real cases of accumulation mode operation, charge transport is anisotropic and Fig. 1a,b suggests that electrochemical doping is spatially inhomogeneous, indicating that only a fraction of the channel volume is actively contributing to conduction. To quantify these effects, the B–M

model was benchmarked against FEM simulations for both planar and vertical device configurations (Fig. 1c). Comparison of the simulated drain current (I_D) and g_m characteristics reveals systematic deviations, which can be also explained by the fact that not the entire channel volume is electrochemically active due to (i) finite ion penetration depth, (ii) contact effects, and (iii) non-uniform electric field distribution across the channel thickness (d). These effects become increasingly pronounced with decreasing channel length (L). Moreover, this limitation becomes evident in Fig. 1c, where the standard B–M model with constant mobility (grey dashed lines) systematically deviates from both FEM simulations and the gate voltage-dependent mobility modified B–M model. Despite the fact that the channel dimensions (d and L) were taken to be the same for the planar and vertical architectures (Fig. 1a,b), the FEM simulation showed different results in I_D and g_m (Fig. 1c). Decreasing L is desirable because it enables higher g_m and faster transistor response, both of which are particularly important for sensing applications. However, L -scaling introduces a trade-off between enhanced switching dynamics and increasingly dominant contact-related limitations.

Our results show that OECT performance is governed by the coupled interplay of geometry, architecture, and transport physics, and cannot be captured by simple scaling laws. These results establish geometry and architecture-aware design rules and highlight the need for V_{GS} -dependent mobility in predictive modeling of CMOS-compatible OECTs.

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