

Deterministic Time-Synchronized Wireless Sensors for Lightweight Flight Test Instrumentation

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Abstract

This paper presents a method for achieving nanosecond-accurate wireless time synchronization of Bluetooth-based sensor nodes aligned to an IEEE 1588 Precision Time Protocol (PTP) Grandmaster. In modern flight test instrumentation (FTI), increasing sensor density and heterogeneous measurements require precise temporal correlation of distributed data sources. While wireless sensors reduce cabling effort and installation complexity, they typically lack deterministic and globally synchronized timing.

The proposed approach enables absolute time synchronization of wireless sensor nodes via a PTP-synchronized gateway and an associated Time Master operating in parallel with the Bluetooth host. The Time Master distributes the global time reference in nanosecond-accuracy to all connected devices, allowing various sensor measurements such as vibration, strain, and temperature to be timestamped with nanosecond accuracy.

Furthermore, a System-on-Chip (SoC) with an integrated Time-Sensitive Networking (TSN) Ethernet interface supporting IEEE 1588 (PTP) and IEEE 802.1AS (gPTP) is introduced. This approach enables further system miniaturization by replacing the gateway, thereby reducing hardware footprint, power consumption, and installation effort in FTI applications.

Key words: Bluetooth, Synchronization, Wireless, PTP, FTI

Introduction

Modern flight test instrumentation (FTI) systems are characterized by an increasing number of distributed measurement points, growing sensor heterogeneity, and strict constraints on weight, installation effort, and system integration. Applications such as structural monitoring, vibration analysis, and thermal characterization require high sensor densities, leading to significant cabling complexity and associated overhead.

Wireless sensor technologies offer clear advantages by reducing wiring effort and enabling flexible sensor placement, particularly in confined or temporary measurement environments. However, their adoption in FTI systems has been limited by the lack of deterministic and globally synchronized timing. Precise temporal alignment is essential to correlate sensor data with avionics signals, control system parameters, and telemetry streams.

In conventional wired FTI architectures, synchronization is achieved using the IEEE 1588 Precision Time Protocol (PTP), providing a common global time reference. While sub-microsecond accuracy can be achieved in wired

networks, transferring this level of determinism to wireless systems remains challenging. Technologies such as Bluetooth Low Energy (BLE) are affected by variable transmission delays, clock drift, and limited timing control.

This paper presents a method for wireless time synchronization with nanosecond-level accuracy of Bluetooth-based sensor nodes aligned to an IEEE 1588 PTP Grandmaster. The approach combines a PTP-synchronized gateway with a dedicated Time Master operating in parallel to the Bluetooth host, enabling deterministic time distribution and precise timestamping of sensor data.

In addition, future integration into TSN-capable SoC architectures is discussed as a path toward further miniaturization and tighter integration into FTI infrastructures.

The main contributions of this paper are:

- Nanosecond-accurate wireless synchronization of Bluetooth sensor nodes aligned to an IEEE 1588 PTP Grandmaster
- A synchronization architecture combining a PTP gateway and a

dedicated Time Master for deterministic time distribution

- Integration of wireless sensors into a globally synchronized FTI environment
- A TSN-enabled SoC concept enabling further system miniaturization and direct synchronization to the global time domain

Requirements

Flight test instrumentation (FTI) systems require deterministic and globally synchronized timing to enable precise temporal correlation of distributed measurement data. Wireless sensor integration introduces additional challenges due to variable transmission latency, oscillator drift, and limited timing control within wireless communication protocols such as Bluetooth Low Energy (BLE).

To ensure compatibility with existing FTI infrastructures, a wireless synchronization approach must fulfill the following requirements:

- Alignment to a global IEEE 1588 Precision Time Protocol (PTP) time reference
- Nanosecond-level synchronization accuracy between distributed sensor nodes
- Deterministic timing behavior with low jitter and stable long-term synchronization
- Compensation of clock drift and oscillator deviations
- Support for precise timestamping of high-frequency measurements
- Compatibility with PTP- and TSN-based measurement networks
- Scalability for distributed wireless sensor topologies
- Low additional hardware complexity, weight, and power consumption

Particularly for applications such as vibration analysis, structural monitoring, and synchronized signal acquisition, insufficient synchronization accuracy directly affects phase relationships and temporal correlation of measured signals. Therefore, wireless synchronization mechanisms for FTI applications must provide both high precision and deterministic behavior comparable to wired IEEE 1588-based systems.

Related Work

Accurate time synchronization in distributed systems is commonly achieved using the IEEE 1588 Precision Time Protocol (PTP), which provides a globally consistent time reference across networked devices. In combination with Time-Sensitive Networking (TSN), e.g., IEEE 802.1AS, deterministic time distribution with sub-microsecond accuracy is well established in wired flight test instrumentation (FTI) systems.

In wireless systems, achieving comparable synchronization performance remains challenging due to variable transmission delays, clock drift, and limited timing control. Existing approaches in Bluetooth Low Energy (BLE) networks typically focus on relative synchronization and are limited to microsecond-level accuracy. For example, Nordic Semiconductor demonstrates a BLE-based timer synchronization method [1] using periodic timestamp exchange and local timer alignment. While effective for relative synchronization, such approaches do not provide deterministic behavior or alignment to a global absolute time reference.

Alternative wireless technologies such as Ultra-Wideband (UWB) enable highly accurate ranging and time synchronization, often achieving sub-nanosecond precision under controlled conditions. However, UWB systems are primarily optimized for ranging applications rather than continuous data transmission. As a result, the effective data throughput for sensor data streaming is typically limited, and system integration requires specialized hardware and increased power consumption, which restricts their applicability in lightweight and resource-constrained FTI environments.

The approach presented in this paper extends existing BLE-based synchronization methods by introducing deterministic and globally aligned time distribution. By coupling the wireless network to an IEEE 1588 PTP Grandmaster via a synchronized gateway and enhancing the synchronization algorithm for improved stability, nanosecond-level accuracy is achieved while maintaining the advantages of low-power BLE communication.

System Architecture

The proposed wireless time synchronization approach enables Bluetooth Low Energy (BLE) sensor nodes to be aligned with the network master clock. In flight test instrumentation (FTI) systems, this master clock is defined by an IEEE 1588 Precision Time Protocol (PTP) Grandmaster, which distributes absolute time and phase information across the measurement network. All distributed sensors, both wired and

wireless, must be synchronized to this reference to ensure consistent timestamping of measurement data. The overall system architecture is illustrated Fig. 1.

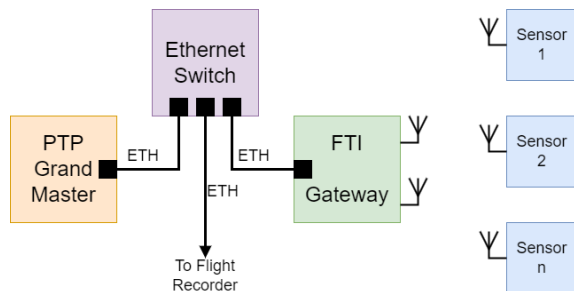


Fig. 1: General Components

The synchronization concept consists of a PTP-synchronized gateway, a dedicated Time Master, and multiple wireless BLE sensor nodes. The Time Master is implemented as an additional embedded device connected to the gateway in parallel with the BLE host. It receives the PTP time and a pulse-per-second (PPS) signal directly from the gateway, ensuring alignment with the global time reference.

The Time Master uses the same radio hardware as the BLE sensor nodes but accesses it directly without passing through the BLE link layer. By bypassing the BLE stack, the transmission of synchronization packets becomes deterministic. The implementation is based on the Multi-Protocol Service Layer (MPSL), which allows the Time Master to utilize free radio timeslots between BLE connection intervals. Within these slots, synchronization packets of 32 bytes are transmitted periodically at 100 Hz on a fixed radio channel.

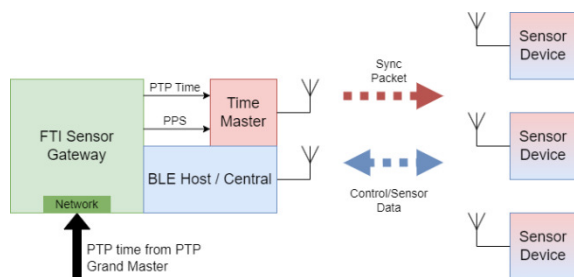


Fig. 2: General Architecture of Time Synchronization

Fig. 2 illustrates the general architecture of the time synchronization system.

BLE sensor nodes use the same mechanism to receive synchronization packets whenever the radio is not occupied by BLE communication. Each node maintains a free-running timer (e.g., 16-bit timer at 16 MHz), which is continuously adjusted to match the Time Master reference. This approach enables deterministic distribution of timing information across all wireless devices.

Synchronization Method

The proposed synchronization mechanism consists of three main components: (i) synchronization of the free-running timers between the Time Master and the sensor nodes, (ii) absolute time synchronization aligned to the IEEE 1588 PTP Grandmaster using PTP time information and a PPS reference, and (iii) an optional alarm mechanism that enables the Time Master to trigger time-synchronized events on the sensor nodes with nanosecond-level precision.

The first component establishes a common time base across all devices by aligning the local free-running timers. This relative synchronization forms the foundation for all subsequent timing operations.

The second component extends this mechanism to absolute time synchronization by mapping the aligned local timers to the global PTP time domain. This ensures that all sensor nodes operate on a globally consistent time reference.

The third component enables deterministic event triggering, allowing the Time Master to schedule and distribute time-critical events that are executed synchronously across all sensor nodes.

The next section describes the synchronization of the free-running timers in detail.

Synchronization of Timers

The synchronization between the Time Master and the sensor nodes is based on aligning two independent free-running timers. Each device maintains a high-resolution free-running timer operating at a fixed frequency (e.g., 16 MHz), which serves as the local time base.

The timer operates in a periodic cycle defined by a compare register (CC):

$$CC[0] = T_{MAX} \quad (1)$$

which triggers a hardware-based timer reset. This establishes a stable and continuous reference cycle for the local timer and ensures deterministic periodic behavior.

To obtain precise timing information, radio events are captured using a dedicated compare/capture channel. Hardware-triggered capture events store the exact timer value at packet transmission and reception:

$$CC[1] \rightarrow \text{timestamp capture} \quad (2)$$

This mechanism enables cycle-accurate timestamping of synchronization packets without CPU involvement and forms the basis for precise offset estimation.

The Time Master periodically transmits synchronization packets containing its current timer value. Upon reception, each sensor node captures the exact arrival timer value using the hardware timestamping mechanism. By comparing the received master timer value with the locally captured timestamp, the sensor node computes the timing offset between its local timer and the reference timer.

The synchronization process compensates for both phase and frequency differences between the two hardware timers. The proposed mechanism is derived from the timer-based synchronization approach described in [1], where timer values are exchanged to align local clocks to compensate for signal phase. While the original method focuses on relative synchronization, it is extended in this work to enable deterministic behavior and improved stability, also for signal frequency.

Phase correction is applied by adjusting the duration of a single timer cycle. Instead of directly modifying the timer value, which would introduce discontinuities, the timer is reset at a shifted compare point:

$$CC[2] = T_{MAX} + \Delta t \quad (3)$$

Where T_{MAX} is the nominal timer period and Δt represents the measured timing offset. Depending on the sign of Δt , the current timer cycle is either extended or shortened, resulting in a smooth alignment of the timer phase.

The correction is executed entirely in hardware using PPI. When the timer reaches the adjusted compare value, a deterministic sequence is triggered: the timer is reset, and the correction logic is disabled automatically to ensure one-shot execution. This guarantees that the phase adjustment is applied exactly once and at a precisely defined time.

In addition to phase alignment, frequency differences between the master and slave timers are compensated over time. Clock drift is estimated from successive synchronization events by observing the evolution of the timing offset. Based on this estimation, the effective timer period is gradually adjusted, reducing long-term drift and minimizing the need for large phase corrections.

By combining phase and frequency correction, the local timer of each sensor node converges with the Time Master reference. The fully hardware-driven implementation ensures deterministic behavior, avoids CPU-induced jitters, and maintains a continuous and monotonic time base.

Absolute Time Synchronization

The synchronization of free-running timers establishes a common tick domain between the Time Master and the sensor nodes. In this domain, all devices share a phase-aligned and frequency-synchronized hardware tick progression. However, these ticks do not directly represent real-world time. To obtain globally consistent timestamps, the synchronized tick domain must be mapped to the absolute time provided by the IEEE 1588 PTP Grandmaster.

The PTP-synchronized gateway provides both the absolute PTP time and a PPS reference signal to the Time Master. The PPS signal defines precise second boundaries, while the PTP time provides the corresponding absolute timestamp. This information is embedded into the synchronization packets and distributed to sensor nodes. Each reference packet contains the hardware tick value at the last PPS event, the corresponding elapsed seconds since a global reference, and the effective number of ticks per second.

Based on this reference, each sensor node reconstructs the current global time by reading the local hardware tick counter, which represents the number of ticks since system start. To ensure consistency, the tick value at the last PPS event and the associated reference seconds are read atomically, preventing race conditions between asynchronous updates and timestamp computation.

The elapsed ticks from the last PPS boundary are computed as:

$$\Delta t_{ticks} = t_{loc} - t_{cap} \quad (4)$$

where t_{loc} is the current timer value and t_{cap} is the tick value recorded at the last PPS event.

These elapsed ticks are converted into fractional time using the effective timer frequency:

$$t_{frac} = \frac{\Delta t_{ticks}}{f_{timer}} \quad (5)$$

The global time is then reconstructed by combining the integer second reference from the PPS signal with the fractional contribution derived from the local tick progression:

$$t_{abs} = t_{pps} + t_{frac} + \Delta UTC \quad (6)$$

For nanosecond resolution, this can be expressed as:

$$t_{abs} = (t_{pps} + \Delta UTC) \cdot 10^9 + \frac{(t_{loc} - t_{cap}) \cdot 10^9}{f_{timer}} \quad (7)$$

where t_{pps} is the number of seconds since the reference PPS and f_{timer} is the effective timer frequency. An optional offset ΔUTC can be applied if required.

The hardware timer frequency is continuously estimated using the interval between successive PPS events. This allows compensation of oscillator inaccuracies and ensures accurate conversion from timer ticks to nanoseconds.

To ensure consistency, PPS-related state variables are read atomically, preventing race conditions between asynchronous PPS updates and timestamp calculations. Additionally, sanity checks are applied to detect desynchronization conditions, such as invalid timer ordering.

By combining hardware-based timer synchronization with PPS-referenced absolute time, each sensor node reconstructs a globally consistent timestamp with nanosecond resolution. This enables precise temporal correlation of distributed measurements within the FTI system.

Deterministic Event Triggering

In addition to time synchronization, the proposed system enables deterministic triggering of events across distributed sensor nodes. This functionality allows the Time Master to schedule time-critical events that are executed simultaneously on multiple sensor devices with high precision.

The triggering mechanism is based on the globally synchronized time base established by the previous synchronization stages. Each sensor node maintains a continuously running local timer that is aligned both in phase and frequency to the Time Master and mapped to the absolute PTP time domain. This synchronized timer serves as a common reference for scheduling future events.

The Time Master embeds trigger information into the synchronization packets, including a target timestamp at which the event shall be executed. Upon reception, each sensor node converts this target time into its local timer domain and programs a hardware compare register accordingly.

When the local timer reaches the configured compare value, a hardware-triggered event is generated. This mechanism relies on direct event–task connections, ensuring that the trigger is executed without CPU intervention and with deterministic timing. As a result, jitter introduced by software scheduling or interrupt latency is eliminated.

The use of hardware-based triggering allows precise alignment of actions such as sensor sampling, data acquisition, or external signal generation across multiple nodes. Since all devices operate on a common synchronized

time base, the trigger events occur simultaneously with nanosecond-level precision.

This capability extends the synchronization system from passive time alignment to active coordination of distributed processes. It enables tightly synchronized measurements and control actions, which are particularly relevant for high-speed and time-critical FTI applications.

Experimental Evaluation

The experimental evaluation was performed using a prototype setup consisting of an IEEE 1588 Precision Time Protocol (PTP) Grandmaster, a PTP-capable Ethernet switch, a PTP-synchronized gateway with an attached Time Master, and a wireless Bluetooth Low Energy (BLE) sensor node.

The gateway was synchronized to the global PTP time domain via the Ethernet network and provided both the absolute PTP time and a PPS reference signal to the Time Master. The Time Master periodically transmitted wireless synchronization packets to the BLE sensor node using direct radio access via the Multi-Protocol Service Layer (MPSL).

To evaluate synchronization accuracy, PPS signals generated at different stages of the synchronization chain were measured simultaneously using a logic analyzer. The following PPS signals were observed:

- the PPS output of the PTP-synchronized gateway,
- the PPS output of the wireless Time Master,
- and the reconstructed PPS output of the remote BLE sensor node.

The synchronization error was determined from the temporal offset between the measured PPS edges. This setup enables direct observation of phase alignment, synchronization stability, and accumulated timing deviations between the wired PTP infrastructure and the wireless sensor node.

Measurements were conducted under controlled laboratory conditions to evaluate the achievable synchronization accuracy and the stability of the proposed wireless synchronization approach.

Measurement Results

This section presents the experimental results of the proposed synchronization system. The measurements focus on the achievable synchronization accuracy between the gateway, the Time Master, and the wireless sensor nodes, as well as the long-term stability of the synchronized time base.

To evaluate the synchronization behavior, PPS signals derived from the synchronized timers were measured using external timing equipment. The following measurements illustrate the temporal alignment between the different synchronization stages of the system.

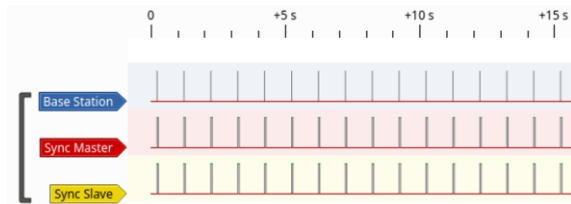


Fig. 3: PPS signals captured by Logic Analyzer

Fig. 3 shows a logic analyzer measurement of three PPS signals within the synchronization system. The first signal (blue) represents the PPS signal of the gateway (Base Station), which is synchronized to the IEEE 1588 PTP Grandmaster. The second signal (red) corresponds to the PPS output of the Time Master (Sync Master), which generates the wireless synchronization packets for the sensor nodes. The third signal (yellow) shows the PPS signal reconstructed on the remote sensor node (Sync Slave).

The logic analyzer was configured with a sampling frequency of 16 MHz, resulting in a temporal resolution of 62.5 ns per sample. The measurement demonstrates that the PPS signals of the Time Master and the remote sensor node remain closely aligned with the gateway reference signal over the observed measurement interval.

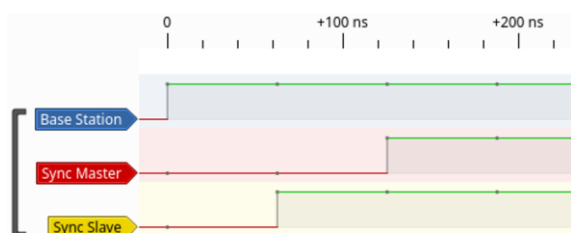


Fig. 4: Phase Shift of PPS signals

Fig. 4 shows a zoomed view of the measured PPS signals from the gateway (Base Station), the Time Master (Sync Master), and the remote sensor node (Sync Slave). The measurement illustrates the remaining phase offset between the synchronized devices at the temporal resolution limit of the logic analyzer.

The observed edge displacement between the PPS signals is within one sampling interval of the measurement system. With the logic analyzer configured to 16 MHz, the temporal resolution is limited to 62.5 ns. Therefore, the remaining

synchronization error between the devices is below the measurable resolution of the setup.

The measurement confirms that the proposed synchronization mechanism achieves highly precise phase alignment between the Time Master and the wireless sensor nodes while maintaining stable synchronization relative to the PTP-referenced gateway signal.

Outlook: TSN-Enabled SoC Integration

The presented synchronization architecture currently utilizes a dedicated gateway and Time Master to bridge the wireless BLE sensor network into the IEEE 1588 PTP domain of the FTI system. As further development, a miniaturized System-on-Chip (SoC) architecture with integrated Time-Sensitive Networking (TSN) Ethernet capabilities is being investigated.

The proposed approach is based on a RISC-V multicore SoC platform, which integrates deterministic Ethernet communication supporting IEEE 1588 PTP and IEEE 802.1AS (gPTP). By combining TSN networking, local processing, and wireless synchronization functionality within a single device, the external gateway infrastructure can be significantly reduced or fully eliminated.

This integration enables further miniaturization of wireless FTI systems while reducing hardware footprint, wiring complexity, power consumption, weight and installation effort. In addition, the deterministic TSN infrastructure allows direct integration into existing avionics and flight test recording networks, enabling compact and energy-efficient next-generation FTI architectures.

References

- [1] A. Fossum, "[Wireless Timer Synchronization among nRF5 Devices](#)," Nordic Semiconductor, Application Note, Jul. 2016.