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A 128-channel Ultrasound Imaging System for High Frame Rate Imaging

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Abstract: Ultrafast ultrasound imaging has opened up new avenues for applications in clinical diagnostics and biomedical research. We developed an open ultrasound platform based on a single FPGA to enable high-frame-rate beamforming. The system comprises a commercial PC for user interaction and an ultrasound acquisition card connected via PCIe 3.0, supporting real-time beamforming and programmable transmission/reception. The parallel delay-and-sum beamformer is implemented using data register shifting technology and can output beamformed images of 128×2048 at a frame rate of 10,557 fps.

Keywords: Beamforming, DAS, FPGA, ultrafast ultrasound, ultrasound system

Introduction

Ultrafast ultrasound technology is increasingly vital for advanced applications like microvascular blood flow imaging and functional ultrasound imaging, fueling the need for higher frame rates in open ultrasound systems [1], [2]. Commercial medical ultrasound systems support various imaging modes but often lack the flexibility needed for research involving custom ultrasound probes. To facilitate advanced ultrasound research, more open and configurable ultrasound platforms are essential. Some commercial open platforms, such as Verasonics, utilize soft beamformers implemented on multi-core CPUs and GPUs[3], [4]. These platforms offer high flexibility and support the development of novel image reconstruction algorithms. Thanks to fully parallel processing, they can even achieve real-time beamforming with frame rates exceeding 1000 fps. However, the performance of soft beamforming is ultimately limited by the data transfer bandwidth of PCI-Express or other high-speed interfaces, as raw RF data must be sent to the host processor for processing.

In contrast, other platforms such as the ULA-OP 256 employ hardware beamformers implemented on field-programmable gate arrays (FPGAs) or application-specific integrated circuits (ASICs)[5]. While hardware beamformers are generally less flexible and harder to modify once deployed, they are capable of much higher frame rates—often surpassing 3000fps—because the FPGA can be directly connected to analog-to-digital converters (ADCs), bypassing the data transfer bottleneck of soft beamforming. Moreover, systems based on FPGA beamforming tend to be smaller, more energy-efficient, and more portable compared to those relying on CPUs and GPUs.

The Delay-and-Sum (DAS) algorithm remains the most widely adopted and straightforward approach for digital beamforming[6]. Although implementing beamforming on a single FPGA simplifies the hardware design of ultrafast ultrasound systems, the need to store a large number of delay values required by the DAS algorithm imposes a considerable burden on FPGA resources. To overcome this limitation, a parallelized FPGA-based DAS architecture has been recently proposed, achieving a beamforming frame rate exceeding 10,000 frames per second for images with a resolution of 128×2048[7].

In this work, we developed a 128-channel ultrafast open ultrasound platform using a single FPGA, and the parallel DAS is implemented in this FPGA. The platform consists of a commercial personal computer (PC) and an ultrasound card, which is connected via PCIe 3.0. The main function of the PC is to interact with users and display information, while the ultrasound card serves as the core component of the platform, enabling beamforming and fully configurable transmission and reception signals. Meanwhile, a sub-aperture 64-channel DAS beamformer is implemented in the FPGA of the ultrasound card. In the beamformer, left and right shifts of the shift register replace the spatial distances between transducer array elements and ultrasound image pixels, enabling parallel DAS beamforming. The beamformer operates at 200 MHz and achieves 10557 frames of image output for 128×2048 images.

Method

Considering a uniform linear array, assuming the pitch of the rectilinear arrays is p, and the total number of array elements is N_X. After beamforming, the image pixel pitch is Ip, j is the j-th pixel,and the

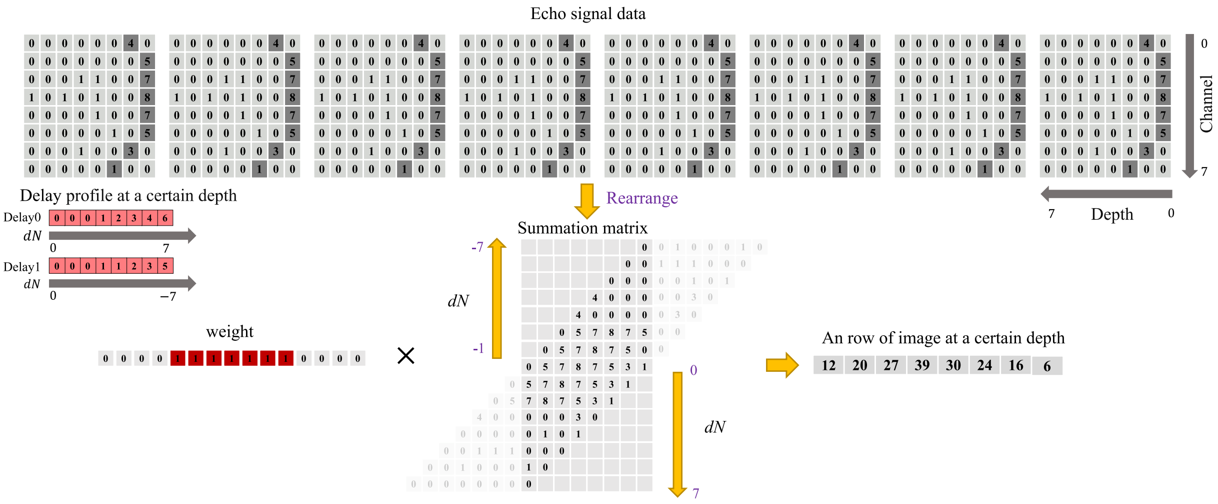


Fig. 1: Schematic diagram of the DAS algorithm for outputting 8 pixels in parallel. Eight copies of the echo signal data sampled from the eight channels are created and stored separately in the memory. Simultaneously, eight delay values at the same depth are read from Delay0 (with positive dN) and Delay1 (with negative dN). Then, the echo signal data are read based on these delay values and shifted left or right according to the corresponding positive or negative dN. Afterward, the processed echo signal data are rearranged in the summation matrix and multiplied by a weight vector related to the sub-aperture. Finally, row summation of the summation matrix is performed to obtain the 8 pixels of the image.

total number of pixels is N_I.The delay value of the parallel DAS with a steering angle θ towards and from a scatterer at $(x,\ z)$ is written as follows:

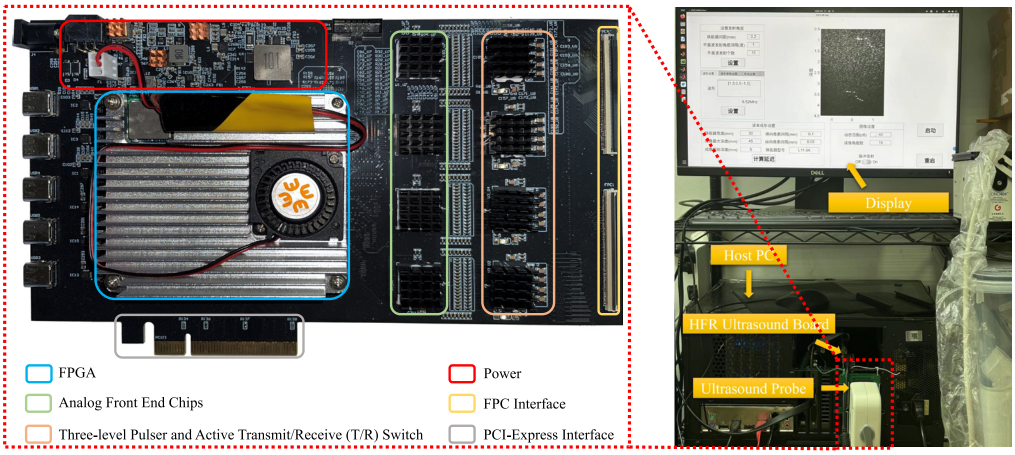
$$\tau\left(dN,z,\theta\right)=\left(z*cos\theta+I_p*dN*sin\theta+\sqrt{\left(I_p*dN\right)^2+z^2}\right)/c \quad (1)$$
$$dN\in\{dN\in\mathbb{Z}|-max(N_X,N_I)\le dN\le max(N_X,N_I)\}$$

Where c is the speed of sound. The detailed implementation method of parallel DAS is shown in Fig. 1. It is worth mentioning that the signals are arranged in a summation matrix, and the rows of the summation matrix represent the sub-aperture sizes. Therefore, dynamic aperture can be achieved by multiplying a weight vector representing the aperture with the summation matrix.

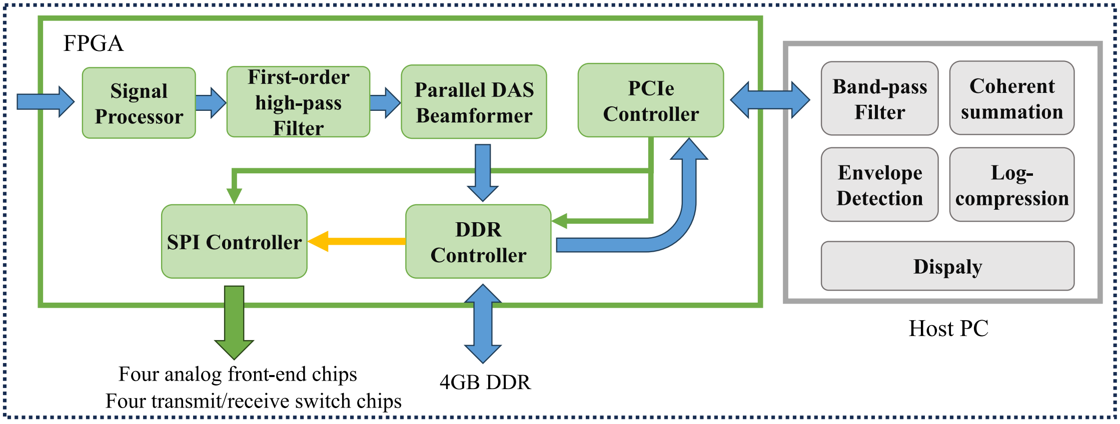
Experiments and results

The hardware architecture of the ultrafast open ultrasound platform is shown in Fig.2. The platform comprises a host PC and an ultrasound card, which is inserted into the PCIe slot on the motherboard, similar to a graphics card. The ultrasound card is based on a single Kintex UltraScale FPGA (XCKU060-FFVA1156-2-I; Xilinx Inc., San Jose, CA, USA). This card leverages four three-level pulser transmit/receive switch chips (TX7332, Texas Instruments) to transmit pulses and four analog front-end chips (AFE5832, Texas Instruments) to receive echo signals. The FPGA independently manages eight chips with a serial peripheral interface (SPI) to control 128 probe elements. The flexible printed circuit (FPC) connector interfaces the probe and the system. Meanwhile, the ultrasound card, measuring 12 cm×21 cm and comparable in size to a standard graphics card, is designed to be inserted into the PCIe slot on the PC motherboard, where the raw RF data or beamformed RF data is transferred via the PCIe (PCIe 3.0 x8) interface to a host PC.

The software architecture of the ultrafast open ultrasound platform is illustrated in Fig. 2. The analog echo signals from 128 channels are sampled by AFE chips and transmitted to the FPGA via the LVDS (Low-Voltage Differential Signaling) interface. On the FPGA, the sampled signals are pre-processed by a signal processor to generate raw RF data. This raw RF data is filtered by a first-order high-pass filter, and the filtered signals are then beamformed by a parallelized DAS beamformer to produce beamformed RF data. Subsequently, the beamformed RF data is stored in an 8 GB dynamic random-access memory (DDR) with a data transfer rate of 153.6 Gbps. Finally, the beamformed RF data is transferred to the host PC through PCIe for generating B-mode images for display. The host PC precisely controls the parallel DAS beamformer and ultrasound chip controller by manipulating registers, providing the system with a high degree of flexibility and configurability. In terms



The hardware photo of the platform



The software architecture of the platform

Fig. 2: The hardware and software architecture of the platform

Tab. 1: Main Parameters of the Platform

General Features	128 independent TX/RX channels; Architecture: ultrasound card + host PC; Ultrasound card size: 12 cm × 21 cm; Display frame rate: 15 fps for 15 angles
Transmitter	Three-level adjustable waveform; Output voltages: ±10 Vpp to ±90 Vpp; Minimum pulse width: 10 ns
Receiver	Analog gain: 12 dB to 51 dB; Programmable DTGC; 12-bit @ 40 MSPS ADCs
Beamformer	Configurable based on probe; Operating frequency: 200 MHz; Up to 15 imaging angles 10,557 fps for 128 × 2048 images.
Operating System	Ubuntu 21.04

of FPGA resource consumption, the largest consumption is from LUT and BRAM, accounting for 40.56% and 70.83% of the total usage, respectively. The main parameters of the platform are listed in Tab.1. In order to further verify the effectiveness of the system, experiments based on a phantom were designed and completed. A 128-element, 6.5MHz commercial uniform linear array, L11-3A, was used to acquire a B-mode ultrasound image of commercial small parts phantoms, Sono404(Sun Nuclear, USA). The PRF was set at 5KHz, and the steering angle was applied with angles ranging from -7° to 7° in 1° increments, for a total of 15 angles. And the sample frequency was set at 26.67MHz, the transmit pulse voltage was set to ±60V. First, the raw echo data is acquired using the platform and uploaded to the PC. Then, the MUST beamforming method is applied on the PC to perform DAS beamforming[8]. Subsequently, beamforming is performed using the platform's parallel DAS beamformer, and the resulting data is transferred to the PC for further processing and display. The final ultrasound images of the phantom are shown in Fig. 3.

As shown in Fig. 3, the differences can be observed between the images generated by the platform and those obtained using the MUST method. Visually, the

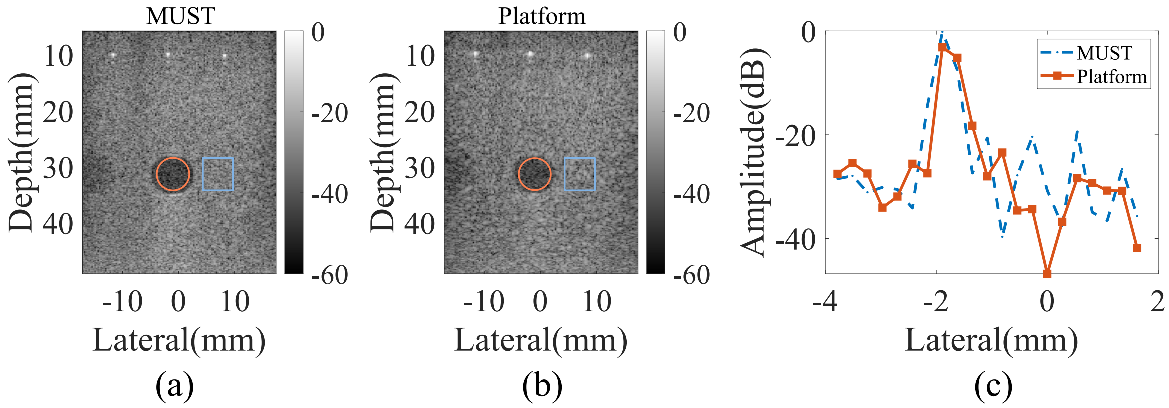


Fig. 3: (a) The results of MUST, (b) results from the platform, (c) the lateral intensity variation of the central strong scatterer.

Tab. 2: The quality of image.

	CR	CNR	FWHM(mm)
MUST	13.77	1.7684	0.3881
Platform	12.00	1.46	0.3375

image quality of the platform output appears somewhat inferior, primarily because the MUST method utilizes full-aperture imaging with floating-point computation, while the platform employs 16-bit fixed-point arithmetic, leading to truncated output values. To further assess image quality, the contrast ratio (CR), contrast-to-noise ratio (CNR), and full width at half maximum (FWHM) are used as evaluation metrics. The region of interest is indicated by a red circle, the background region by a blue rectangle, and the FWHM is calculated based on the central strong scatterer. The results are presented in Tab.2.

Conclusion

In this work, we developed an ultrafast ultrasound imaging platform based on a single FPGA, with a parallel DAS beamformer implemented directly on the hardware. Phantom experiments demonstrate that the image quality of the platform output is somewhat lower than that of the MUST method. However, the platform achieves a significantly higher frame rate. The observed image degradation is acceptable for most applications. Overall, the proposed ultrasound platform is capable of performing ultrafast imaging effectively.

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