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Design and Technology for Cavity SOI Piezoelectric Micromachined Ultrasonic Transducers (PMUTs) with an Infinite Cell Array Design.

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Abstract: Piezoelectric micromachined ultrasonic transducers (PMUTs) using aluminum nitride (AlN) as the active piezoelectric layer represent a powerful and compact alternative to conventional bulk piezoelectric elements. Due to their CMOS compatibility, high mechanical robustness, and strong potential for miniaturization. This paper presents a detailed insight into the design and fabrication and characterization of PMUTs utilizing cavity SOI technology and a unique infinite cell design for improved channel shape and size development.

Keywords: PMUTs, Cavity, SOI, AlN, Cell

Introduction and Motivation

Ultrasound technology is currently undergoing a fundamental transformation, shifting away from bulky, discrete components toward highly integrated, miniaturized systems [1], [2]. In particular, micromachined ultrasonic transducers (MUTs) are enabling entirely new applications in the fields such as medical imaging technology, automotive systems, and consumer electronics due to their compact design and low-voltage electronics integration.

MUTs generate acoustic signals using thin film membranes; these signals can be analyzed through reflection and interaction with objects for both imaging and actuation/sensing purposes. When arranged in arrays, MUTs enable spatially resolved detection and high-resolution ultrasound and photoacoustic imaging [3], [4].

The development of piezoelectric MUTs provides powerful, CMOS-compatible alternatives to traditional bulk piezoelectric elements. AlN has proven to be a particularly well-suited active piezoelectric material, offering excellent thermal stability, low dielectric losses, and outstanding process compatibility with modern silicon technologies [3], [5], [6], [7] [8].

The PMUTs presented in this paper are based on cavity SOI-based membranes and utilize AlN for the generation and detection of ultrasound signals. Fabricated using well established, wafer-based MEMS processes, they enable highly miniaturized, scalable, and cost-effective production. Due to their compact size, low operating voltage, and high integration capability, these PMUTs are ideal for use in portable devices, industrial inline measurement systems, as well as in medical diagnostic equipment.

Operating Principle

PMUTs consist of numerous oscillating membranes that generate ultrasonic waves. Their operation is based on the unimorph principle, wherein a piezoelectric layer is sandwiched between top and bottom electrode and is bonded to a thin, silicon membrane. When an electrical voltage is applied, the membrane deforms due to the inverse piezoelectric effect, generating ultrasonic waves. In contrast, an incoming acoustic wave causes mechanical deformation which is then converted into an electrical signal [2], [7], [8]. This dual functionality enables both the transmission and sensing of ultrasound signals. Figure 1 shows the cross section of a PMUT, after applying a signal between the top and bottom electrode.

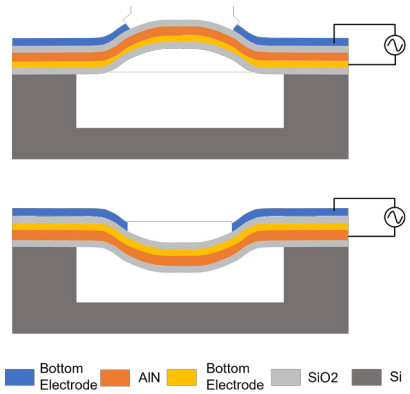

Fig. 1: Cross-section of a PMUT showcasing the operating principle

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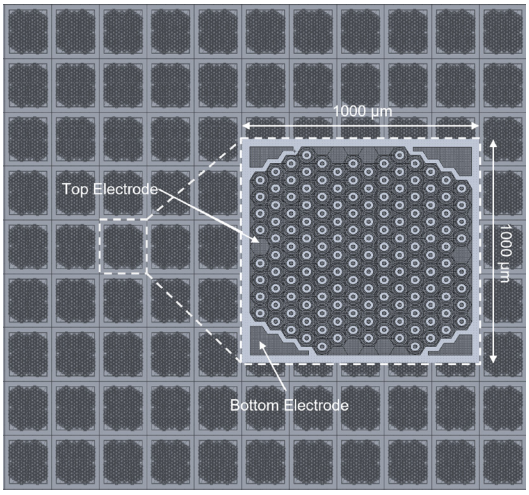

Fig. 2: The design of a PMUT cell array with an enlarged PMUT cell and dimensions

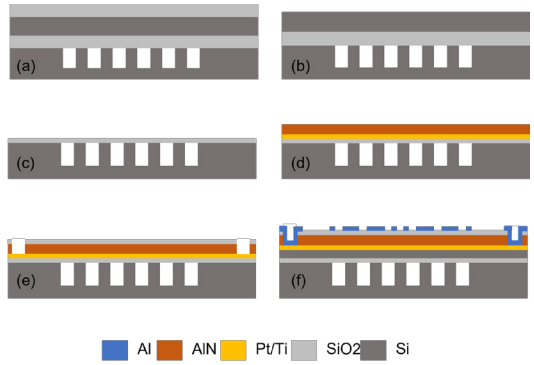

Fig. 3: Process flow of PMUTs for formation of cavities (a) Wafer Bonding (b) Si grinding and etching (c) SiO2 wet etching (d) Deposition of Ti/Pt and AlN (e) via etching for contact to bottom electrode (f) Al depostion and patterning

PMUT Design

A key innovation of this work lies in its patented cell architecture, which offers a high degree of application flexibility. These PMUTs wafer consist of numerous individual cells structures of 1 x 1 mm², each comprising 150 circular membranes. Each PMUT cell can be operated independently or interconnected via wire bonding to form arrays. By adapting the wire bonding layout, the geometry, size, and number of acoustic channels can be freely configured without requiring any changes to the silicon chip design itself. Whether a linear, circular, or complex array configuration is needed, the PMUT chip can be easily tailored to the specific application using automated wire bonding technology.

This post-fabrication reconfiguration of the channel layout enables fast prototyping and modular system integration. The design of the PMUT cell array is shown in Figure 2, The figure shows a small part of the wafer along with a enlarged sketch of the individual PMUT cell. The Four corner areas act as the contact for bottom electrode whereas the top electrode covers the full center area of chips (except for the membranes). The top electrode covers 60 % of the total membrane area for optimal output.

Fabrication

The fabrication of PMUT cells is carried out on two 150 mm wafers which are then bonded together using direct bonding. The PMUTs were fabricated using a simple three mask process.Figure 3 shows a cross-sectional representation of the fabrication process. The fabrication process begins with the deposition of the resist to create cavities in the handle wafer. The resist is then patterned accordingly, followed by DRIE process for etching 25µm Si. These cavities define the position of each PMUT membrane. For the device wafer fabrication, the process begins with the growth of 3 µm thermal oxide on both sides of the Si.

The bonding of the two wafers was performed using direct bonding. To find the optimum bonding parameters the wafers were bonded at room temperature both in atmospheric pressure and in vacuum, step (a). The wafers are then subsequently annealed at 1000 °C to enhance the bond strength and the quality of the interface between the bonded wafers. Figure 4 presents IR images depicting the conditions of the wafers before and after annealing, specifically for those bonded through direct bonding at room temperature in vacuum and under atmospheric pressure.

After bonding, the SiO2 is etched using a wet etch process, step (b). The wafer is then thinned down until 40 µm Si is remaining on top of the SiO2 using a grinding step. This Si is then removed using a dry etching process. The 3000 nm SiO2 is further reduced down to 1500 nm using wet etching forming a thin SiO2 membrane on top of the cavities, step(c).

The Ti/Pt stack is subsequently deposited using a PVD process. 20 nm Ti is deposited which functions as an adhesion layer between Pt and SiO2, while the 100 nm deposited Pt serves two functions, it acts primarily as the bottom electrode for the PMUTs as well as functions as a seed layer for the AlN. Then 600 nm AlN is deposited using PVD, step (d). A thin layer of SiO2 is deposited using PE-CVD, this SiO2 layer acts a hard mask for the AlN etching.

After the SiO2 deposition, the second mask is used to define vias to the bottom electrode through dry etching of the SiO2 and AlN, step (e). Once the vias are etched a final 500 nm of Al top electrode is deposited. In the final step the thrid mask is used

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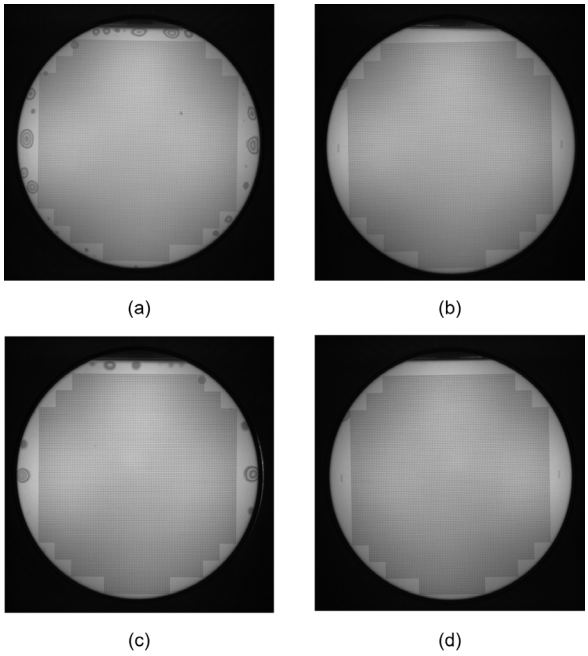

Fig. 4: IR Images of the PMUT wafers after bonding at (a) atmospheric pressure and (b) in vacuum and post annealing IR images of wafers bonded at (c) atmospheric pressure and (d) in vacuum

to pattern the top electrodes of PMUTs. The Al is etched using a wet etch process, step (f). PMUTs with a membrane diameter of 50 µm were fabricated with an overall cell size of 1000 µm x 1000 µm. An optical microscope image of part of the fabricated PMUT array form the wafer is shown in Figure 5.

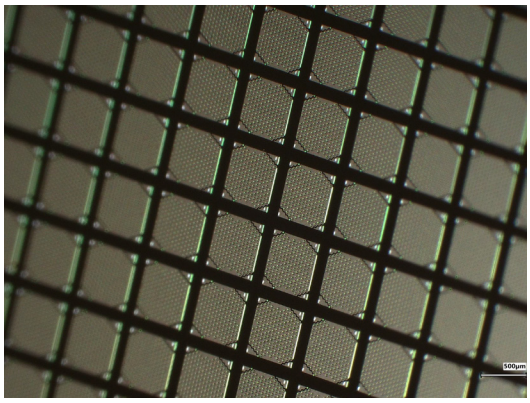

Fig. 5: A microscopic image of a part of a fabricated array from a PMUT wafer

Characterization

The wafer-level electrical characterization of a PMUT cell arrays was carried out.The out-of-plane membrane deflections are recorded at the center using a Polytech

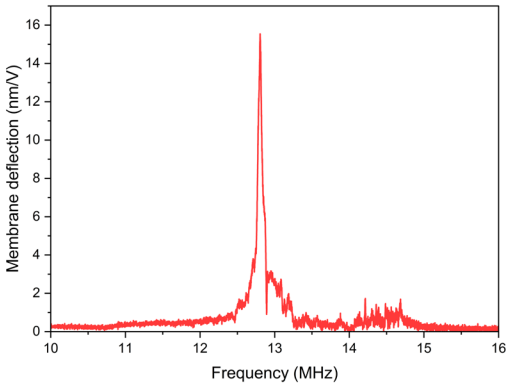

Fig. 6: LDV measurement for the membrane delfrction and frequency of the PMUTs

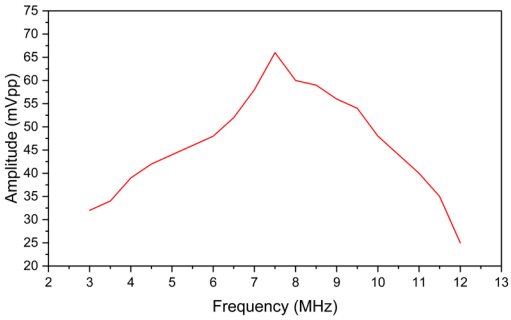

Fig. 7: The Frequency vs Amplitude plot of the PMUTs in an oil bath.

MSA-100 3DLaser Doppler Vibrometer (LDV) with an ACTR-110 axis controller. The PMUTs were actuated with a chirp signal with a voltage amplitude of 1 V and the resonance frequency as well as the membrane deflections were recorded.

These PMUTs exhibit a resonance frequency of around 12.7 MHz in air with a out of plane membrane deflections of 14 nm/V. The resonance frequency varies slightly over the wafer with a standard deviation of 3.1 %. The dynamic membrane deflection of the PMUT membrane is plotted in Figure 6. The electrical capacitance of each cell over the wafer is measured using a an automatic prober (Karl Suss PA-200) and an LCR meter (Keysight, E4980A) and was found to be around 57 pF.

The transmit performance of the PMUT array was measured using an acoustic hydrophone (Müller Instruments, Germany) in an oil bath. A 3 mm x 1 mm linear PMUT array was fistly diced, mounted and wire bonded to a PCB. The PMUT linear array was excited by connecting it to the function generator and actuating it with a square burst wave of 5 cycles of 10 V and the frequency response was recorded at 10

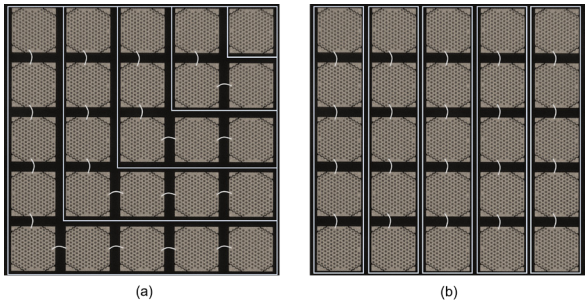

Fig. 8: Wire bond plans for (a) Matrix arrangement of cells (b) linear arrangement of cells

mm. The output of the hydrophone was connected to an oscilloscope through a preamplifier. The maximum pressure was recorded at 7.5 MHz. Figure 7 shows the frequency vs amplitude of PMUTs in Oil.

Modular Chip and Cell array design

A significant advancement of this technology is its PMUT cell architecture, which provides extreme flexibility for various applications. As the entire wafer consists of numerous PMUT cells, allowing for flexible chip configuration and customized form factors by adapting custom wafer dice plans. Furthermore, each PMUT cell can function independently or be connected through wire bonding to create various array shape and size.

By adapting the wire bonding layout, it is possible to customize the geometry, dimensions, and quantity of acoustic channels without necessitating alterations to the design of the silicon chip. The PMUT chip can be readily adapted to accommodate various configurations, including linear, circular, or intricate arrays, utilizing automated wire bonding technology. This ability to reconfigure the channel layout after fabrication facilitates rapid prototyping and supports modular system integration. Figure 8 show two of these custom array geometry.

Conclusion

The design, fabrication and characterization PMUTs based on cavity SOI platform with an infinite cell design was discussed in this paper. A simple 3-mask fabrication process for the development of AlN based PMUT was developed and PMUTs with 50 µm membrane diameter were successfully fabricated. This cavity SOI-based process enables fabrication of smaller diameter membranes, overcoming the challenges of high aspect ratios faced in traditional DRIE-based Si back etching for small membranes.

The post fabrication mechanical electrical and acoustic characterization was carried out to evaluate the performance of the PMUT cell arrays. These PMUTs exhibit a resonance frequency of 13 MHz in air and the frequency shifts to 7.5 MHz in liquids with an overall bandwidth of 110 % in liquids. The capacitance/cell of the PMUTs is 57 pF.

The advanced PMUT cell architecture design offers exceptional flexibility in chip configuration, enabling the customization of acoustic channels without altering the silicon chip design. This adaptability allows for the creation of various array shapes and sizes, facilitating rapid prototyping and seamless integration into modular systems.

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