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Design and Integration of Functional Blocks for Sub-THz Radar Sensor Systems up to 300 GHz

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Abstract

Taking advantage of modern semiconductor processes and advanced integration technologies, the operation frequencies of fully integrated systems are continuously rising. The wide bandwidth available in the mm-wave and in the sub-THz frequency domains paves the way to various sensing applications. However, the design and integration challenges also increase with the complexity of such systems as well, often resulting in long development cycles. This paper highlights the functional block developments within the iCampus LausiTHz[1] project on radar sensor systems in D- (110-170GHz) and J-bands (220-325 GHz). By developing integration-ready RF blocks, transceiver ICs, and antennas as well as the capability of heterogenous integration, the project aims to enable faster development of such complex systems.

1 Introduction

The advantages of modern radar systems such as contactless measurement, operation in harsh environments, and all-electronic operation have led to new sensing applications. Exploiting modern semiconductor processes [1] and advanced packaging technologies, operating frequencies are continuously rising. Recent exploitation can be seen for in-vehicle sensing [2] and 3D imaging [3]. Operation of radar in the mm-wave and sub-THz spectrum, makes larger bandwidth available, increasing range resolution and reducing component size. However, with increasing frequencies, available output power and efficiency decrease while RF losses increase. In addition, using a larger bandwidth increases the severity of parasitic effects on RF signal paths and antennas. Therefore, output power and gain must be improved and integration losses minimized, while taking all electrical effects in the design of RF signal paths and antennas into account. There are already radar sensors and frontends available up to 240 GHz as system-on-chip integrating multi-channel transceiver and antennas [4]. While the on-chip integration of components allows a compact frontend, a compromise has to be found between the performance of transceiver and antenna, as well as the overall chip size. An alternative is the heterogeneous integration, combining various RFICs of different technologies and components in a single package [5]. In this paper, overview of the research conducted on the design of sub-THz transceiver and amplifier RFICs, on-chip antennas as well as the use of heterogeneous integration of SiGe and InP technologies for the realization of frontends and package-integrated antennas within the LausiTHz project is presented. The goal is to develop and evaluate technological building blocks usable for a faster development of future heterogeneously-integrated radar sensors.

2 Transmitter ICs

The 160 GHz transmitter (TX) assembly consists of a combination of a SiGe-based TX IC and an InP-based power amplifier (PA) chiplet flip-chip mounted onto it. This integration step is realized by a dedicated technology with micro bumps that offers bandwidth well beyond 200 GHz [5]. The SiGe IC is designed using the advanced IHP SG13G3 technology, which is based on [1], providing a transit frequency (f_T) of 510 GHz and a maximum oscillation frequency (f_{max}) of 600 GHz. It consists of a driver amplifier (DA) operating at Ka-band, a D-band frequency quadrupler, and a filter followed by a D-band DA feeding the InP PA chiplet, and a series of couplers and power detectors, before and after the InP PA for built-in monitoring of input and output power levels. The overall block diagram of the envisioned TX assembly is shown below in Fig. 1.

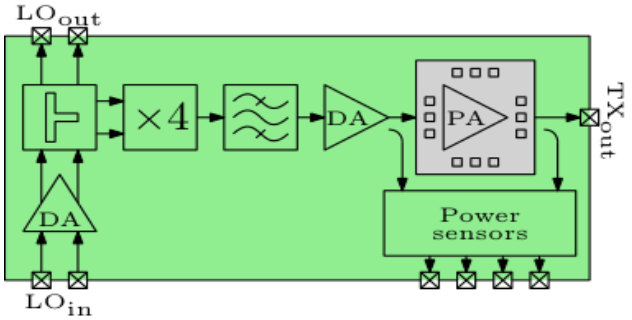

Figure 1 Block diagram of the D-band TX assembly with the SiGe TX IC (green) and InP PA chiplet (grey)

The SiGe TX IC is built based on the LO-scalable architecture [6], [7], allowing the number of TX channels to be expanded across the LO signal chain. This begins at the LO input port, where an external signal source provides a 39.5 GHz input signal. This signal is amplified and then

1 Funded by Federal Ministry of Research, Technology and Space of Germany (BMFTR) within project iCampus Cottbus.

split by a coupler into two paths. One path is routed to an output pad to facilitate LO scalability, while the other path feeds the on-chip frequency multiplier chain. Within the multiplication chain, the signal passes through a frequency quadrupler converting the signal to D-band, followed by a band-pass filter and a DA. To ensure integrity, the DA output is monitored by a power detector after a 20-dB coupler. Finally, the InP PA chiplet provides high-power amplification. The signal is transferred back to the SiGe IC at the output of the chiplet. The signal is sampled again with another 20-dB coupler to monitor the output power. The thru loss of the coupler is optimized to avoid degrading the TX output power. This configuration ensures that the signal is filtered, multiplied, and amplified to the necessary power levels while providing the readout mechanism required for real-time monitoring of the D-band output. A breakdown at building block level is given in Table I. The target bandwidth is at least 10 GHz.

Parameter→ Building Block↓	**IP1dB (dBm)**	**Gain/CG (dB)**	**PDC (mW)**
LO Driver Amplifier (DA)	−11	20	80
D-band quadrupler	5	−13.5	15
D-band DA	−3	11	20
Power detector	−15	-	1

Table I Expected parameters of the D-band TX IC

The D-band PA is realized as a 3-stage design based on InP HBTs with 700 nm emitter width. Each stage is based on a differential stacked common-base topology with respective baluns at the input and output. Below, Fig. 2 presents the layout of the RFIC. It is designed in an inverted microstrip architecture to avoid detuning by the flip-chip assembly. The simulated RF output power is approximately 17 dBm.

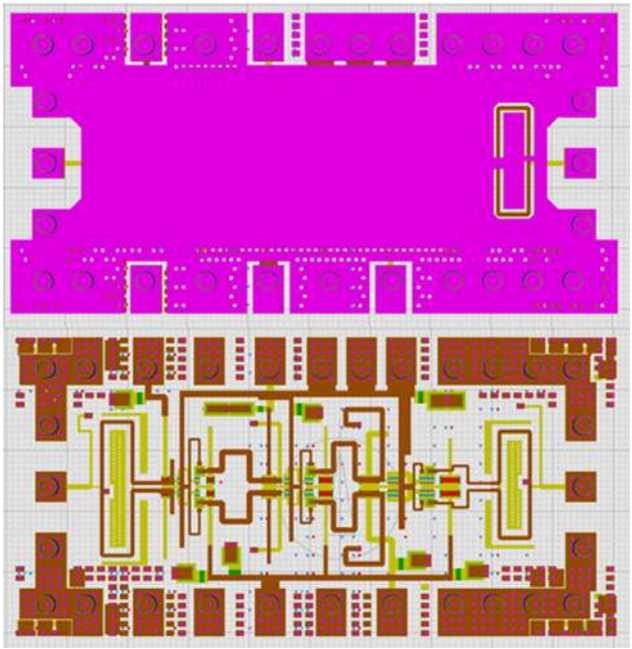

Figure 2 Layout of InP PA, top layer (top) and layer below top (bottom).

The J-band TX IC (Fig. 3 right), is also designed in the IHP SG13G3 technology, targeting an RF bandwidth of more than 50 GHz. An external LO source, provided by the RX IC counterpart, around 35 GHz drives the input. The LO signal undergoes a series of amplification stages in the Ka- and D-bands and frequency multiplication factors of 2 and 4. The doubler output at J-band is amplified by a 3-stage PA and radiated into air through on-chip antennas. The design is made fully differential for its desirable characteristics especially at sub-THz frequencies.

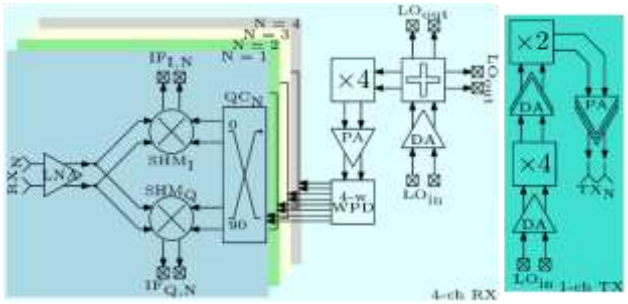

Figure 3 Block diagram of the J-band RX and TX ICs

The expected performance parameters of the functional blocks of the J-band TX are tabulated below (Table II). A power close to 15 dBm is expected at the antenna input with total simulated power consumption of 650 mW.

Parameter→ Building Block↓	**IP1dB (dBm)**	**Gain/CG (dB)**	**PDC (mW)**
LO Driver Amplifier (DA)	−4	12	10
D-band quadrupler	7	−10	15
D-band DA	−5	10	35
J-band doubler	4	0	20
J-band PA	−7	21	550

Table II Expected parameters of the J-band TX IC

3 Receiver ICs

The 160 GHz receiver (RX) IC is also designed in the IHP SG13G3 technology and features four channels. The RX IC mirrors the LO-scalable architecture of the TX, utilizing the same source. The IC consists of the same multiplication chain as the TX. Its output is converted back to differential signaling by means of a low-imbalance low-loss balun and amplified further by a D-band differential amplifier, feeding the LO ports of four quadrature RXs, after a 4-way power dividing structure. Each RX includes a quadrature coupler, two mixers, and an LNA with an integrated power divider (Fig. 4). On the RF signal end, each RX features an LNA providing 20 dB of simulated gain and only 5 dB of simulated noise figure. The incoming RF signal is split by a power divider to feed both quadrature mixers. The down-converted IF signals are routed to the output pads. This modular architecture allows for straightforward scaling of the number of elements in a RX array. Each RX chain is expected to have about 35 dB of overall conversion gain.

The J-band RX IC (Fig. 3 left), is designed in the IHP SG13G3 as well, targeting again an RF bandwidth of at

least 50 GHz. In contrast to the D-band version, the scalable RX IC at J-band has two LO outputs, one for cascading multiple RC RFICs, and the other for an LO source to the TX counterpart. The LO signal undergoes additional amplification after a multiplication chain similar to the TX to drive four quadrature RX channels. In contrast to the D-band RFIC, here the mixers are operated in a sub-harmonic manner, as it is more energy-efficient to obtain sufficient LO power. Expected performance of the functional blocks of the J-band RX are tabulated below in Table IV. The LO chain is expected to consume around 165 mW and each RX channel about 175 mW. An overall conversion gain of 22 dB is expected with a noise figure of only 11 dB.

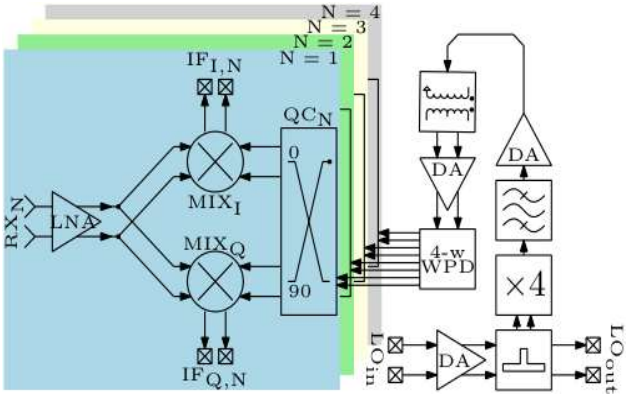

Figure 4 Block diagram of the D-band 4-channel RX IC

Parameter→ Building Block↓	IP1dB (dBm)	Gain/CG (dB)	PDC (mW)	NF (dB)
LO DA	−1	13	90	-
Quadrupler	5	−13.5	15	-
SE DA	−3	11	20	-
DE DA	−1	13	90	-
LNA	−19	20	35	5
Mixer	−12	20	5	8

Table III Expected parameters of the D-band RX IC

4 Antennas

4.1 On-Chip Antennas

On-chip antennas are the preferred choice for the J-band radar system. Integrating the antenna directly with the active circuit eliminates lossy transitions. The short wavelength at this frequency also allows miniaturization, making it easier to include the antenna on the chip [8].

Parameter→ Building Block↓	IP1dB (dBm)	Gain/CG (dB)	PDC (mW)	NF (dB)
LO DA	−4	12	10	-
Quadrupler	7	−10	15	-
DE DA	−4	12	70	-
LNA	−13	14	135	10
SHM	−9	11.5	20	17

Table IV Expected parameters of the J-band RX IC

The mentioned SiGe technology enables this integration, which offers excellent high-frequency performance. On the other hand, off-chip antennas for this frequency range suffer from severe signal loss and impedance mismatch due to package interconnects. The flip chip with solder bumps requires complex compensation networks to function properly while standard wire bonds generate high parasitic inductance levels [8], [9]. The design of on-chip antennas is also challenging, as the very thin metal layer in the standard back-end-of-line process results in a smaller spacing between the radiation element and the ground plane, which degrades antenna efficiency and bandwidth. Moreover, silicon has a high relative permittivity of around 11.9 and low resistivity, leading to significant energy dissipation and poor radiation efficiency. Due to the high dielectric constant in silicon, surface waves may be generated, which can distort the radiation pattern [10]. To overcome the challenges a micromachining post-processing technique known as localized backside etching (LBE) can be used. The lossy, high-permittivity silicon is removed under the radiating antenna element by LBE, effectively reducing conductive losses. This also suppresses the excitation of the surface wave. Therefore, an on-chip antenna with LBE significantly improves the radiation efficiency [9], [11].

4.2 On-Package Antennas

For the radar system at D-band, off-chip antenna options are evaluated, since the parasitic effects are not as severe. Various on-package antenna arrays at D-band (cf. Fig. 5) are analyzed based on an 127µm thick RF PCB substrate (Isola Astra MT77). Numerical simulations are performed to design the arrays and optimize the radiation performance.

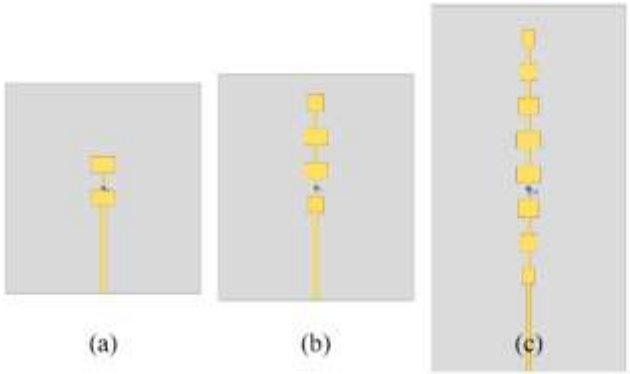

Figure 5 Design of 1×2, 1×4, and 1×8 antenna arrays

Antenna	1×2 Patch	1×4 Patch	1×8 Patch
Substrate	Isola Astra MT77 (ε_r 3, tanδ 0.004)		
Bandwidth	9.4 GHz	7.6 GHz	12.7 GHz
Return loss	40.9 dB	36.0 dB	60.2 dB
Gain	10.1 dBi	12.4 dBi	14.8 dBi
Beam width	17°	12°	7°
SLL	−11.1 dBc	−16.6 dBc	−15.2 dBc

Table V Simulated performance of various antenna arrays

Table V below gives a comparison of the simulated performance results for the patch antenna arrays. All designs show sufficient bandwidth and good matching in the frequency range of interest. With increasing array size, the antenna gain increases while the beam width decreases, as expected.

5 Integration

A PCB-based integration technology for the realization of the D-band frontend-antenna interface is investigated. For the IC interconnects, flip-chip and wire bond options are compared using numerical simulations. The 3D models used for EM simulations are shown in Fig. 6 and Fig. 7. The simulations results of flip-chip and wire bond transitions show sufficient RF performance in the frequency range of interest. The simulated transition and return losses are indicated in Fig. 8 and Fig. 9, respectively.

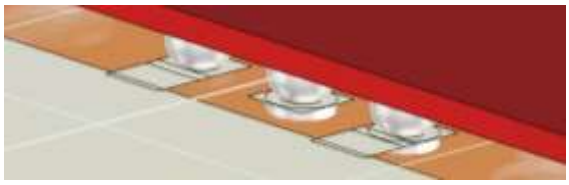

Figure 6 EM simulation model of Flip-chip transition

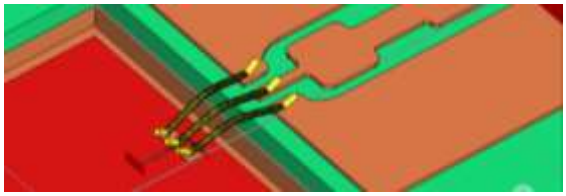

Figure 7 EM simulation model of wire bond transition

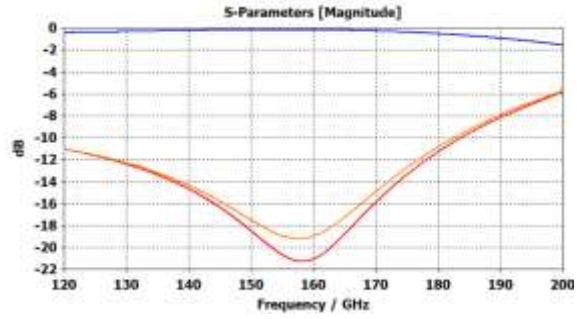

Figure 8 EM simulation results for flip-chip transition

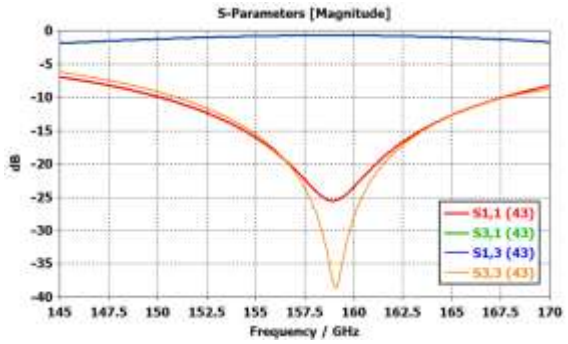

Figure 9 EM simulation results for wire bond transition

6 Summary and Outlook

Components and integration technologies for realizing sub-THz radar systems were investigated. The J-band radar system is planned to integrate at least three of each of the TX and RX ICs in the LO-scalable manner, where on-chip antennas are utilized. The D-band radar system is envisioned combining SiGe and InP technologies to take advantage of the capabilities of both domains. Expected results from the SiGe-based ICs, InP-based PAs, on-chip antennas, and PCB-based antenna arrays show promising simulated RF performance for the targeted sub-THz radar applications in the automotive and imaging domains.

7 References

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