DOI 10.5162/SMSI2025/P42

Neuromorphic Spiking Sensory Conversion System Based on the STDP Learning Rule of Biological Synapses

Hamam Abd [1], *Anand Joshy*[1] *and Andreas König*[1]
[1] Lehrstuhl Kognitive Integrierte Sensorsysteme (KISE), EIT, Rheinland-Pfälzische Technische Universität Kaiserslautern-Landau, 67663 Kaiserslautern, Germany
habd@rptu.de

Summary: Developing a standard sensory system using advanced integration technologies presents both advantages and obstacles due to issues like noise, manufacturing deviations, and signal swings. Adopting a self-adaptive approach and shifting from traditional amplitude-based processing to a biologically inspired, adaptive spike-domain framework provides a practical solution. This work introduces a neuromorphic model of an adaptive spiking sensory front-end featuring self-X properties and capacitive storage. A learning loop enables continuous synaptic updates to prevent signal degradation, using spike-timing-dependent plasticity (STDP) for adaptation.

Keywords: Spike-domain code, STDP learning rule, self-X properties, Neuromorphic spiking sensory system

Background, Motivation and Objective

Sensory systems are rapidly evolving, with advances in transduction and integration enabling miniaturization and diverse applications, simplifying use but complicating electronic design [1]. Modern mixed-signal systems enhance efficiency and speed with lower voltages and capacitance but challenge traditional analog designs with increased noise, reduced signal amplitude, variability, mismatch, and lower gain. Reliable analog front-ends (AFEs) are critical for system performance, requiring robustness, accuracy, and self-X features like self-healing, self-calibration, and self-optimization. Fig. 1 shows a typical sensor interface with signal conditioning, amplification, filtering, and ADC. PGAs boost weak signals for ADC range, anti-aliasing filters reduce noise and align signals, and the ADC digitizes them for processing.

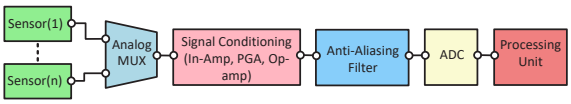

Fig. 1: The conventional AFE system chain.

Traditional AFEs relied on amplitude-coded signals, but modern CMOS technology's reduced transistor sizes and supply voltages shift the focus to time-coded signals, offering better adaptability and robustness. To address these limitations, we developed a neuromorphic spiking sensory system with adaptive capabilities, combining spike timing and an approach inspired by acoustic localization (Fig. 2) [2]. The system uses an adaptive synapse model with a CMOS-emulated memristor to mimic biological synapses [3] and was fabricated with XFAB CMOS 0.35 μm technology, featuring a self-adaptive spiking sensory front-end [4]. Previous systems used counters to control adaptive synapse weights [2]. This study replaces counters with capacitive storage, requiring periodic refreshing. A learning loop based on STDP, inspired by auto-zeroing techniques, reduces adaptation variables and transistors count compared to the previous implementation by using the counters, while enabling dynamic refreshing to prevent value degradation.

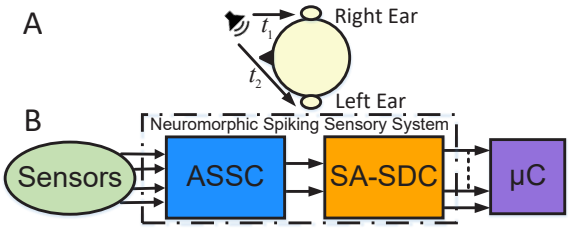

Fig. 2: A block diagram of neuromorphic spiking sensory systems, incorporating ASSC and SA-SDC.

Proposed Methodology and Results

The proposed neuromorphic spiking sensory system uses an adaptive sensor signal-to-spike converter (ASSC) and a self-adaptive spike-to-digital converter (SA-SDC), as shown in Fig. 2. The ASSC converts sensor signals into two spikes with a time difference (TD) representing the sensor output, while the SA-SDC generates digital codes from the TD. The ASSC aligns the SA-SDC input range with the sensor output through time-domain amplification and level shifting, avoiding data loss or costly range expansion. The SA-SDC comprises the Self-Adaptive Spike-to-Rank Coding (SA-SRC) and the Winner-Take-All (WTA) mechanism, as shown in Fig. 3. The SA-SRC encodes timing differences via spike order coding, based on spike

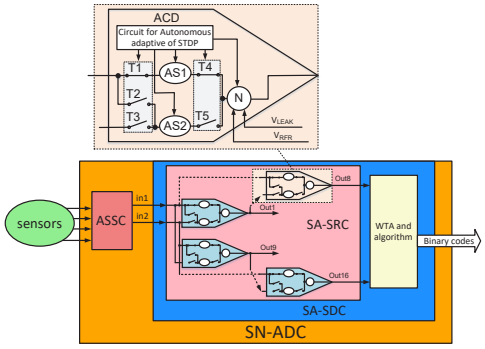

Fig. 3: The proposed neuromorphic AFE based on STDP adaptation

sequences in a neuron group. The WTA converts these patterns into digital signals. At its core, the SA-SRC uses an Adaptive Coincidence Detector (ACD) with two adaptive synapses (AS) and a neuron (N). The delay chain duration depends on the neuron's firing time, influenced by input current intensity and adjusted synaptic weights to match timing variations.

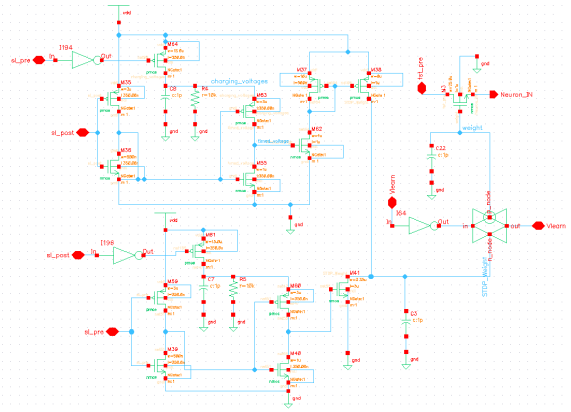

Fig. 4: Schematic of the proposed synapse.

Biological synapse models aim to replicate natural functions [6], but often require many adaptation parameters and transistors. For our ACD as a neural network time delay based on the STDP rule, we focused on key features. STDP, vital for learning and brain function, adjusts synaptic weights based on the timing difference between pre-and postsynaptic spikes [5]. The direction of weight change depends on whether this timing difference is positive or negative, continuing until the target weight is reached. We modified and optimized existing synapse models [6] to enable ACD to operate as a time delay element within a neural network using the STDP learning rule, as illustrated in Fig. 4. The STDP circuit has two sections: potentiation (top) and depression (bottom). Resistor-capacitor pairs set the time constant. The capacitor C3 influences the gate voltage of PMOS M3 by charging capacitor C22 during active learning. Once learning ends, C3 disconnects, leaving C22 directly linked to the PMOS gate. The synaptic weight controls neuron firing delay, adjustable between 3.7 ns and 11.6 ns by influencing the neuron's membrane capacitor charge.

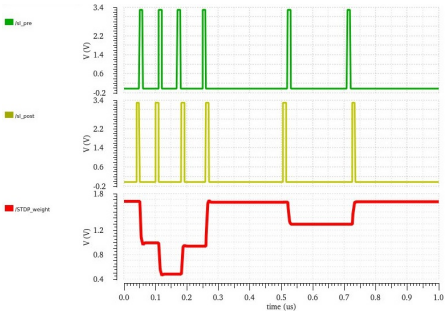

Fig. 5: The synaptic weight adjustments

The autonomous circuit regulates synaptic weights by leveraging pre- and postsynaptic spikes alongside the nominal delay. This adjustment occurs simultaneously across all ACDs by managing switches T1, T2, T3, T4, and T5. As a result, the adaptation time remains independent of the number of synapses since all are updated concurrently. In each ACD, the circuit adjusts the first synapse's weight by connecting it while disconnecting the second. Similarly, the weight of the second synapse is adapted in parallel. Fig. 5 illustrates the synaptic weight adjustments based on pre- and postsynaptic spikes. In the current phase of the design, pre- and postsynaptic spiking events emulate the generation and adaptation of pre-and postsynaptic spikes in the planned complete circuit. The next phase focuses on developing an autonomous circuit to control these events, marking the first step toward a physical demonstrator or chip.

References

[1] Luo, Yifei, et al. "Technology roadmap for flexible sensors." ACS nano 17.6 (2023): 5211-5295.

[2] Abd, Hamam, and Andreas König. "Design of a CMOS memristor emulator-based, self-adaptive spiking analog-to-digital data conversion as the lowest level of a self-x hierarchy." JSSS, 2022. 233-262.

[3] Abd, Hamam, and Andreas König. "Adaptive Spiking Sensor System Based on CMOS Memristors Emulating Long and Short-Term Plasticity of Biological Synapses for Industry 4.0 Applications." tm-Technisches Messen 88.s1 (2021): s114-s119.

[4] Abd, Hamam, et al. "Neuromorphic Spiking Sensory System with Self-X Capabilities." IEEE Access (2024).

[5] Gerstner, Wulfram, and Werner M. Kistler. Spiking neuron models: Single neurons, populations, plasticity. Cambridge university press, 2002.

[6] Bahuguna, Yash, et al. "32nm CMOS Analog Circuit Implementation of STDP for SNNs." 2023 14th ICCCNT. IEEE.