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AI and other Trends in MEMS Industry Change the Foundry Models

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Summary:

AI requires drastically increase in computing power, which is not primary limited by the processors, but two other factors:
1.) Core to core communication, which will switch from electronic to optical data transfer to overcome current issues. Here a fundamental change from silicon- and silicon nitride-photonic to lithium niobate and similar is happening. The later one is incompatible with CMOS technology, shifting photonic from ASIC to MEMS foundries. The according customers request design- and product-support, increasing the foundry responsibility beyond pure wafer processing, which is a significant step for MEMS foundries.
2.) Computing power is throttled due to overheating, requiring new cooling concepts. Beside water cooling of the racks, decentralized local cooling will be necessary. Here MEMS will play a key role due to low cost, power consumption and size, resulting in a multitude of designs and process flows for individual solution per processor as discrete element or integrated with the µprocessors. Here and in many other cases, it is obvious, that the standardized process approach as copied from ASIC foundries is not successful. The wafer process reflects the mutual optimum of customers-design and -requirements and foundry capabilities. The trend for integrated MEMS-cooling, inertials with an ASIC cap, pMUT and medical fluidics on ASIC, etc reflects the merge of CMOS, MEMS and assembly processing [1]. This drives pure-play MEMS foundries to extend their scope. Additionally, MEMS-on-ASIC accelerates the 300mm transition of MEMS to be compatible with the advanced CMOS nodes.

Keywords: AI, MEMS foundry, medicals, TFLN photonic, CMOS compatibility, 300mm.

Introduction

In the early days of MEMS it became obvious, that the ASIC foundry approach of pre-defined and standardized processes is not useful in MEMS industry, resulting in one-product-one-process methodology. With pMUT technology, the standardized MEMS process flow had a short revival, which now again disappears. So, today the typical approach is the cooperation of a fabless customer with a specialized MEMS foundry for a tailor-made process on 150 or 200mm wafers [2], where the foundry is only responsible for the wafer processing. All of that is subject to change due to recent industry trends.

Photonic

Silicon- and silicon nitride-photonics are CMOS compatible and require tight CD control. Consequently, they are fabricated primarily in CMOS foundries using high end lithography. The upcoming thin film lithium niobate TFLN [3] and similar materials do not comply with CMOS wafer processing, they will be produced in MEMS foundries. But the according customers expect design support or predefined design libraries, a PDK and a standardized process flow. The design ownership let the clear separation of foundry (only process-responsibility) and a device supplier vanish, because the design & process ownership results in a product performance responsibility. The foundry must extend its scope or partner with a design house and share the responsibility.

Medicals

Fluidic devices and probe holder for medicals are not real MEMS, since no mechanical-electrical functionality is given. However, as specialty semiconductors they are produced in MEMS foundries, because those are used to tailormade solutions. But medical devices bring their own and very specific requirements to the MEMS fab. Biological compatibility drives new contamination monitoring concepts as well as unusual materials and coatings.

DNA sequencing is a challenge by itself, since very small line width may be combined with materials, which are not CMOS-compatible. Here a drive to 300mm may occur to get access to ArF lithography for the required CDs despite relatively low volume [4].

MEMS with ASIC as cap, ultrasound-transducers- and other MEMS-on-ASIC

Several companies with different devices evaluate an ultrasound transducer to be built on the CMOS on wafer level. Another approach uses the ASIC as a cap for the MEMS [5]. We see for many more cases a strong tendency to MEMS-on-ASIC technology. In all those cases, beside alignment, chip size and chemical compatibility, the wafer size of ASIC and MEMS must match. Switching to a smaller ASIC node drives the need for 300mm MEMS processing also for device types, where the wafer volume doesn't justify such leap. For many customers / devices, the generation 1 is a discrete element, whereas the later generations are MEMS-on-ASIC. This factor has increasing importance for the foundry choice.

MEMS Cooling

The µprocessor calculation power is more and more limited by overheating. The current macroscoping cooling solutions will be extended or replaced by MEMS cooling [6]. Those technologies may drive stacking of the actor wafer with interposers for in- and outlet of air, generating chaotic turbulences, etc.. Integration of cooling MEMS on CMOS or system in package solutions may be the subsequent step. This is another factor of merging MEMS-, CMOS- and assembly processing.

Extended defect monitoring and full or partial wafer level test at the foundry

Defect sensitive devices drive extended monitoring. But on one hand it is not commercially useful to scrap all wafers with a defect; on the other hand, it is too expensive to install an additional defect monitoring at the customer to fish dies with killing defects. Therefore, it is useful to 1.) adapt the defect monitoring to the specific product requirements and 2.) transfer the available defect information per wafer to the customer, like position and criticality based on defect type and size as inkmap. Consequently, 1.) foundry and customer have to partner openly and 2.) the foundry takes over responsibility for the functionality of single devices on the wafer. Similar is valid, when the foundry does apply electrical wafer test of the devices.

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