

Chip-scale Electrochemical Angular Accelerometer based on SOI Substrate

Maoqi Zhu^{1,2}, Yulan Lu^{1,2}, Bowen Liu³, Deyong Chen^{1,2}, Junbo Wang^{1,2}

¹ Aerospace Information Research Institute, Chinese Academy of Sciences, Beijing 100190, CHINA,

² University of Chinese Academy of Sciences, Beijing 100049, CHINA

³ Minzu University of China, Beijing 100081, CHINA

jbwang@mail.ie.ac.cn

Summary:

This paper reports a chip-scale MEMS electrochemical angular accelerometer (EAA) based on an SOI substrate, featuring a monolithically integrated microchannel and sensitive electrodes. By employing 3D plate electrodes with a reduced 10 μm gap, redundant silicon area is minimized. Enhanced high-frequency sensitivity and lowered noise levels are achieved within a compact $10 \times 10 \times 1.5 \text{ mm}^3$ footprint, making the device well-suited for unmanned aerial vehicle (UAV) attitude detection and control.

Keywords: Electrochemical angular accelerometer, SOI, Chip-scale integration, 3D plate electrode, UAV attitude detection and control.

Background, Motivation and Objective

Angular acceleration detection is the core foundation for achieving stable flight and safe control of unmanned aerial vehicles (UAVs). However, UAV angular acceleration is primarily detected through gyroscope differentiation, which suffers from high latency and low accuracy. While miniaturized electrochemical angular accelerometers (EAAs) [1-3] have been proposed, they are often hindered by rapid sensitivity decay and high noise levels. In this work, an SOI-based EAA is presented that overcomes depth-to-diameter ratio limits. By significantly reducing anode-cathode spacing, the device achieves enhanced bandwidth and high-frequency sensitivity. Furthermore, the optimization of planar electrodes into 3D plate structures minimizes redundant area and lowers the noise floor, effectively addressing the inherent limitations of conventional EAAs.

Description of the New Method or System

A chip-scale sensor microfabrication process utilizing an SOI substrate (300- μm handle / 2- μm buried oxide (BOX) / 40- μm device layer) is proposed. Initially, deep reactive ion etching (DRIE) is performed on the backside to remove the handle layer, followed by reactive ion etching (RIE) of the BOX layer to create through-silicon vias (TSVs). Subsequently, a Ti/Pt bilayer is sputtered for electrode metallization. By leveraging the 40 μm SOI device layer to surpass conventional etching constraints, 3D plate electrodes are defined by DRIE, enabling a significant reduction in anode-cathode spacing from 50 μm to

10 μm . Finally, the processed SOI substrate is bonded to a glass lid through anodic bonding, and the device fabrication is completed by sputtering metal into the electrode vias.

Results

Experimental results show that the proposed EAA achieves a peak sensitivity of 1 V/(rad/s²) at 0.01 Hz, featuring improved high-frequency response and broader bandwidth. Furthermore, the noise level is reduced to $4.52 \times 10^{-6} \text{ rad/s}^2/\sqrt{\text{Hz}}$ (-106.90 dB) at 1 Hz, significantly outperforming the reference devices in Tab 1. The noise reduction stems from optimized anode-cathode spacing, enhanced convection suppression by 3D plate electrodes, and the parasitic-free SOI substrate. These findings offer a valuable reference for developing high-performance miniaturized inertial sensors for drone and aircraft platforms.

References

- [1] Zaitsev D L, Agafonov V M., Precession Azimuth Sensing with Low-Noise Molecular Electronics Angular Sensors. *Journal of Sensors* 2016, 6148019 (2016), doi: 10.1155/2016/6148019.
- [2] T Liang, Z Sun, Microelectrochemical Rotational Vibration Sensor With SOI-Based Microelectrodes Used for Seismic Monitoring, *IEEE Transactions on Instrumentation and Measurement* 73, 1-8 (2023), doi: 10.1109/TIM.2023.3330213.
- [3] M Zhu, J Wang, Chip-Level Packaged Electrochemical Angular Accelerometer with a Wide Measurement Range, *IEEE Sensors Journal* 25, 18941-18951 (2025), doi: 10.1109/JSEN.2025.3561182.

Figures

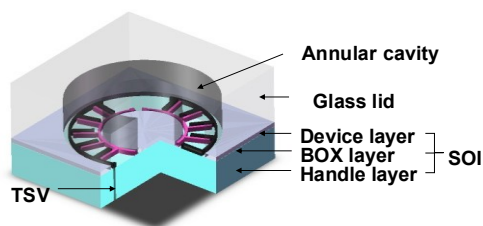


Fig. 1. Diagram of chip-scale EAA based on SOI substrate.

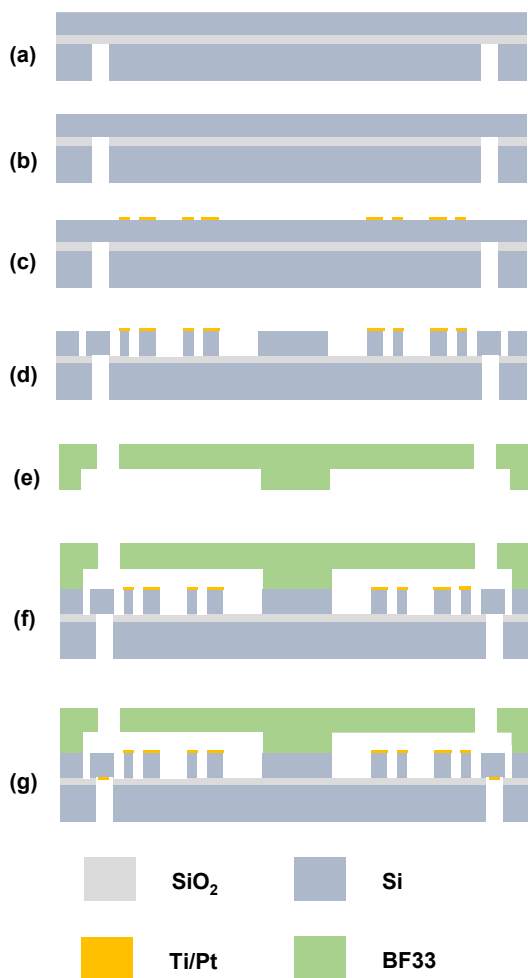


Fig. 2. Fabrication process of the proposed chip-scale EAA.

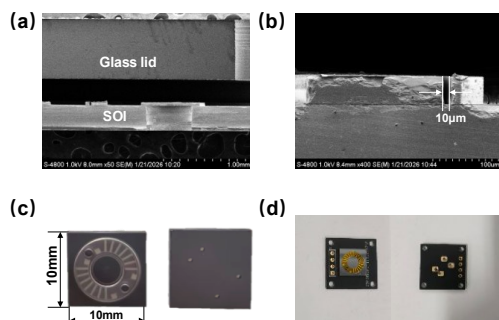


Fig. 3. SEM diagram and physical image of the proposed chip-scale EAA.

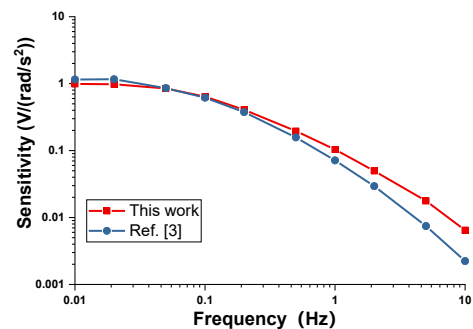


Fig. 4. Graph of sensitivity vs frequency for this work and Ref. [3].

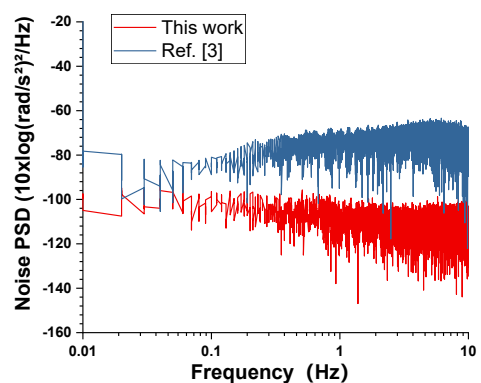


Fig. 5. Graph of Noise Power Spectral Density (PSD) vs frequency for this work and Ref. [3].

Tables

Tab. 1: Performance comparison of the chip-scale EAA fabricated in this study with other devices.

	[1]	[3]	This work
Sensitivity (V/(rad/s ²))	0.5	1	1
Linear range (°/s ²)	297	500	500
Noise level at 1Hz ((rad/s ²)/√Hz)	10 ⁻⁴	7.94×10 ⁻⁶	4.52×10 ⁻⁶
Size(mm ³)	Φ 9×7	10×10×1.5	10×10×1.5

Acknowledgement

This work was funded by the Deep Earth Probe and Mineral Resources Exploration - National Science and Technology Major Project under grant 2024ZD1002503, in part by the National Natural Science Foundation of China under Grant 62571516, Grant 52335012 and Grant U23A20362, in part by Beijing Natural Science Foundation under Grant 4242012, in part by the Youth Innovation Promotion Association CAS under Grant 2023134.