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A new packaging approach for reliable high temperature MEMS devices based on multilayer ceramic interposers

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Abstract

In this work, we will describe a promising procedure for the development of a silicon based micro electro mechanical system (MEMS) suitable for 300°C operation temperature. Design aspects as well as a suitable packaging concept and technology will be highlighted. The value of accompanying FEM simulations together with the usage of novel reliability tools will be demonstrated as a design and construction accelerator that can help to avoid typical mistakes within the material selection and concept phase of a MEMS fabrication process. We will give an introduction for suitable wafer-level-bonding methods for multilayer stacking of functional substrates especially for the heterogeneous integration of silicon and low temperature co-fired ceramic LTCC. The fabrication process for LTCC with electrical feed troughs and for Silicon substrates with through silicon vias TSVs and a subsequent electrical interconnection between both will also be topics of this work.

Key words: LTCC, wafer-level-bonding, high temperature, MEMS, packaging, reliability

Introduction

Miniaturized sensor and electronic solutions can be found anywhere in our modern live. Supporting production flows by delivering relevant process data like temperature, pressure, moisture, ph-value and many more, MEMS and accompanying electronics became essential for various branches of industry due to their high precision and low cost aspects. Furthermore, ongoing miniaturization and the increasing in integration are key elements for consumer, medical and information technology applications to allow MEMS such as microphones, inertial sensors, visual sensors, to be part of every modern smart phone, camera, and laptop / tablet computer. To open further application scenarios, 3-D integration promises highest degrees of functionality within smallest packages contemporary with wireless data transmission and power supply.Although small size, high functionality and low cost of such integrated systems are very favorable a weakness can still be identified when it comes to harsh environments. Current packages already enable hermetical sealing providing protection from moisture, dust and particles. They are also capable of shielding from radiation and mitigate mechanical influences from the surrounding environment. However, many risks still exist when packages are facing high temperatures, high pressure, acidly environmental fluids, or high mechanical or radiation introduced stresses. These challenges need to be tackled by new package designs, the usage of new materials, and by developing new integration processes. Besides allowing the desired functionality, the new packages need also to assure proper manufacturability and high reliability of the heterogeneous systems at the same time. Therefore, package development is key to opening new fields of applications to future MEMS and electronics systems.

With this work, we present the initial steps of the development towards a technology platform that allows a MEMS including TSVs produced by silicon micromachining to be bonded to an LTCC interposer that redistributes the electrical interconnects to the system terminals at the backside of the interposer. The MEMS is a multi-functional sensor. It comprises an array of electrostatic cells capable of receiving and transmitting ultrasonic sound as well as temperature and pressure sensors. This MEMS is supposed to operate at 300°C service temperature. Hence, the package with all its parts and interconnects need to be stable up to this high temperature and bring the electrical signals reliably to the backside where the signal processing die is situated. Within this concept,

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the US cells of the MEMS will directly face the harsh environment whereas most of the other parts can be protected by the package. Still, the entire system will be exposed to the high temperature.

The integration scheme starts with zero-level-packaging to join two silicon substrates under vacuum to fabricate the sensor itself on wafer-level. Afterwards, a second wafer-level-bond (WLB) generates the joint between the MEMS and LTCC substrate (Fig.1).

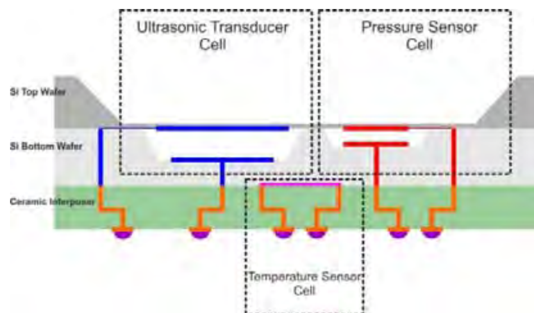

Fig. 1. Schematic Sensor Design as a cross-section view.

Comprehensive Fabrication Workflow

Based on the specification deduced from the application scenario, the components are designed to fulfill their function and the materials are selected to comply with the service conditions. In addition, FEM simulations are performed to assess the thermo-mechanical situation during fabrication and service of the sensor system. Based on engineering test samples, reliability studies are conducted to physically probe the suitability of all relevant components for the use at 300°C. The experimental results will then be used to also validate the outcome of the simulation and to establish lifetime models. Altogether, the comprehensive set of test samples, reliability testing, physical failure analysis, and numerical simulation establishes a design for reliability process. It will lead to the selection of the right materials and the most suitable fabrication processes. In addition, it makes virtual prototyping methodologies available to the actual product development phase so that design optimization can be based on simulation rather than requiring more long-lasting tests. The proposed workflow for the sensor fabrication is schematically shown in Fig. 2

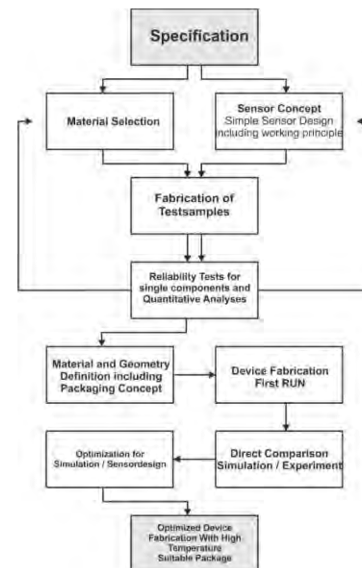

Fig. 2. Schematic work flow for a sensor fabrication as a design for reliability approach

Design process

Simulations for high temperature stable systems - general approach

The simulation of the assembly processes and the high temperature service situations are aiming at the following six objectives:

a) Quantitative analysis and evaluation of the thermo-mechanical loading conditions;

b) Identifying potential weak points in the design of the components such as allowing undesirable distortions and high thermo-mechanical stresses to occur during fabrication and/or operation of the new components;

c) Contribution to the understanding of the effects of aging and failure mechanisms, to be seen during the operation of the high-temperature components;

d) Proposing optimum geometry, material, and process parameters to increase yield and robustness of the production process and to ensure the reliability of the products;

e) Generating, evaluating, and verifying correlative relationships between the thermo-mechanical stress parameters (including fracture mechanical parameters) and the experimentally determined lifetimes – i.e., exploration of lifetime models;

f) Providing methods for 'virtual prototyping', i.e., for the pre-optimization of the design solutions regarding manufacturability and reliability of the high-temperature components based on numerical

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simulations rather than by practical tests only.

In the above list of objectives a) ... f), the complexity of the simulation tasks and the demands on the precision of the underlying models are continually rising. To comply with these demands, a sequence of three stages can be distinguished in the simulation work flow:

Stage 1: Quantitative analysis and evaluation of the general loading situation

- Geometries are modeled based on CAD data;
- Material data is applied as it is available in open literature or pre-existing databases;

This input allows a first assessment and the performance of systematic parameter studies. This way, the most important factors concerning the thermo-mechanical risks for manufacturability and reliability can be determined. The location of the potential weak points within the future components and the significance of the individual factors can be assessed.

Stage 2: Detailed analysis of the most important aspects concerning the manufacturability and reliability of the complete system

- Inclusion of real geometries and identification of critical material parameters (including those of process dependent properties) for which dedicated characterization measurements are performed;
- Involving fracture or damage mechanics concepts – e.g., by applying the virtual crack closure technique (VCCT), the cohesive zone method (CZM), and the extended FEM (X-FEM);

This stage allows quantifying the key parameters and provides precise trend forecasts for lifetime and reliability.

Stage 3: Verification of the simulation results and validation of the virtual prototyping schemes

- Verifying the calculated displacements, strains, and mechanical stresses with innovative 2-D and 3-D measurement methods;
- Validation of the simulation results based on the observed failure mechanisms, the actual fault location, and time sequence of the real failures;

Direct comparison between the simulation and the experimental results is the basis for the development of virtual prototyping methodologies and schemes. Ultimately, they deliver prognosis results based on simulation that are as precise and trustworthy as the practical results of experimental sample tests but obtained in a fraction of time.

Materials and Technologies

In order to achieve a system suitable for harsh environments and high operation temperature, all materials involved have to be selected carefully. The use of silicon as a sensor material has many advantages regarding processability. By selecting advanced metallization systems, all requirements of the high operation temperature can also be met very well. Advanced low temperature co-firing ceramic (LTCC) substrates offer coefficients of thermal expansion close to silicon, so that these two materials can directly be joined even at elevated process temperatures. The bonding itself may require a few intermediate layers or can even be done directly [1]. For the presented demonstrator, the electrical interconnects between MEMS and interposer will be through substrate vias to ensure electrical interconnection as well as mechanical robustness and hermeticity.

Silicon Multi-Sensor with Vias

Silicon micromachining offers various options for generating movable elements and required 3-D structures at micro-scale. Typical metallization technologies can be applied together with etching and lithography processes to form the electrical paths, pads, and electrode needed for the sensor systems. On top of patterned silicon and some deposited functional layers, they allow forming the electrostatic actuators and all the sensing elements of the multifunction sensor platform.

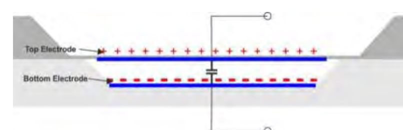

Fig. 3. Capacitive sensing / actuation principle

To enable highest functionality at minimal size, through silicon vias are used to connect the top and bottom electrodes with the backside of the sensor. Fig. 4 shows the process flow for TSV preparation in principle. The suitability of standard electro chemical deposition (ECD) processes for generating the Cu vias has been show with sample structures on 6" wafers.

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Subsequently, reliability tests will be performed to assess the stability of the via/die interface.

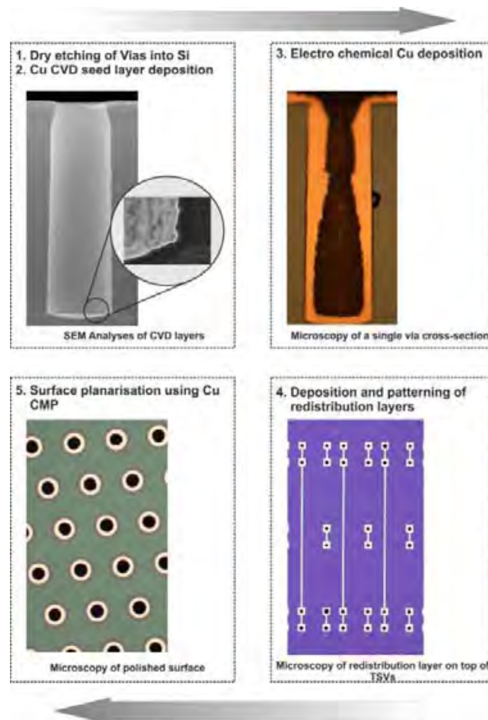

Fig. 4. Process flow for TSV integration.

Starting with dry etched holes with diameters of 30 µm and 50 µm into silicon substrate, the subsequent thermal oxidation of the silicon leads to a film of 1 µm thickness that provides good isolation from the substrate. Then, copper seed layer is generated by chemical vapor deposition with 50 nm thickness at the bottom of the via (Fig. 5).

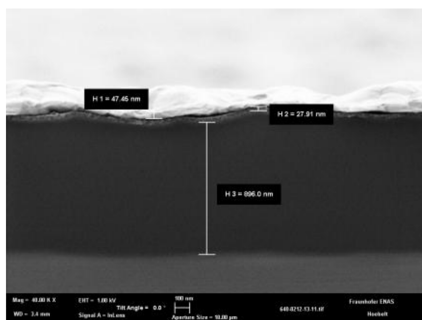

Fig. 5. SEM Analysis: Bottom of TSV with 50 nm Cu Seedlayer. Adhesion-/Barrier Layer and thermal Oxid is visible.

The following Cu ECD process led to partially filled Cu TSV. These almost conformal films induce much less stress into the silicon as fully filled TSVs despite the large mismatch in thermal expansion between Cu and Si (Tab. 1). After dicing the wafers, the samples are ready for reliability evaluations in terms of thermal cycles and high temperature storage. SEM Analyses will show the suitability of Cu TSVs for a high temperature MEMS.

Tab. 1: CTE comparison

Material	CTE in[10^{-6}/K]
Silicon	3
Copper	17
Platinum	9
Tungsten	4.5

By comparing the CTE of possible materials for electrical feed troughs for MEMS, Pt and W were considered as alternatives to Cu TSVs. The electrical properties are adequate. Hence, the final decision on the TSV material will be made after completing the reliability tests. Currently, the assessment is ongoing.

LTCC Subtrate with Vias

In standard LTCC manufacturing process (Fig. 6), the ceramic substrates comes in form of flexible tapes. It is structured by punch and laser processes to form vias, cavities, and channels. Subsequently, the vias is filled with conductive paste to make the vertical electrical connection. The conductor layouts is printed on the unfired tapes either using screens or stencils. These processed layers are stacked and laminated together, before they are are sintered to compact, monolithic modules at 850°C in a furnace. At this stage, the microelectronic components can be assembled and all connections to the external terminals can be made. Finally, the panels containing multiple devices are singulated by sawing. Because of its multilayer processability, LTCC is more flexible and more suited for high volume production at lowest cost than alternatives like borosilicate glass wafers which usually is used commercially for anodic bonding of MEMS so far [2].

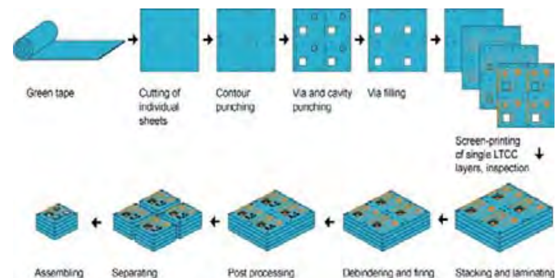

Fig.6 LTCC Manufacturing Process[3]

In this work, a new LTCC tape is applied. It has special anodic bonding properties and comes with a CTE as low as 3.4 ppm/K to match the CTE of silicon very closely. The very low roughness of Ra < 100 nm of the LTCC surface and the wafer flatness of <10µm/20 mm leads to obtain optimum bonding results especially for anodic bonding [4]. Applying pressure assisted

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sintering technology (PAS), the post-firing polishing steps and to increase the surface quality of the LTCC can be minimized. Therefore, the LTCC substrates in the sintering furnace are fired at 850°C and pressed up to 2 MPa. A steady uniaxial pressure inhibits the in-plane shrinkage of the tapes and minimizes the surface roughness. Sticking between the pressure plate and the LTCC is avoided by non-sintering alumina tapes or setter plates like glassy carbon plates [5]. Fig. 7 shows the first promising results in terms of roughness and wafer flatness after the sintering of the anodic bondable LTCC tapes.

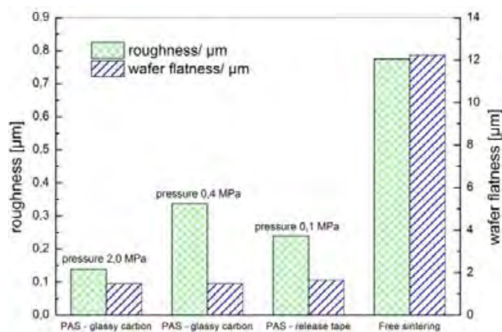

Fig 7: Results on roughness and sheet resistance measurements

The average wafer flatness Wa < 2 µm/ 20 mm of all tapes sintered by PAS process could be highly decreased in comparison to free sintered tapes (Wa ~ 12.2 µm/ 20 mm). Furthermore the roughness of the PAS processed tapes is significantly brought down to Ra ~ 0.14 µm (glassy carbon setter) compared to tapes of the free sintering process with a average roughness of Ra ~ 0.78 µm. Further experiments with optimized parameters should improve the wafer roughness close to anodic bonding specifications (Ra < 0.05 µm).

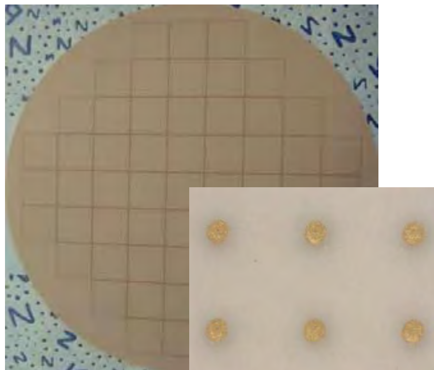

Fig 8: 200 µm Vias integrated in LTCC-Wafer

Fig. 8 shows an anodic bondable 4" LTCC wafer for thermocompression bonding tests. It has a test structure of integrated 200 µm gold vias (81 Vias per cm²) and bonding frames of 100 µm width. The wafer thickness is 0.4 mm after sintering with the PAS process. The vias were punched and filled with gold paste by stencil printing. The bonding frames made of copper paste are printed by screen printing. A minimum via diameter of 50 µm can actually be achieved.

Packaging Technologies

LTCC and Si are joined by wafer-level packaging as it is well known for MEMS packaging. This zero level packaging approach enables highest throughput due to the fact that every device is packaged simultaneously. However, the numerous electrical vias in both parts make this process quite challenging requiring precise placement and low shrinkage. The subsequent dicing step generates the individual devices.

Criteria's that have to be fulfilled by the bonding step are: mechanical robustness, electrical interconnection, hermetic sealing (at least for the MEMS) and suitability for 300°C operation temperature.

In this work we will compare copper thermo compression bonding and anodic bonding as suitable WLB technology to match the above mentioned criteria's. Whereas for anodic bonding mainly the presence of Na Ions and low roughness are key factors for successful bonding, Cu TKB relies on pretreatments to remove oxids from the surface and high temperature and pressure during bonding [6],[7].

Tools for High Temperature Reliability Investigations

Practical reliability investigations are besides FE simulation an essential part for the lifetime assessment of e.g. MEMS components. They are usually performed by means of accelerated lifetime tests, which basically emulate the real life stress pattern under artificial conditions, followed by comprehensive failure analyses. Acceleration can be realized by conscious modification of specific test parameters, such as the increasing of the test temperature. However, the challenge is to ensure the same failure modes like being found in real life operation at the same time.

In case of typical MEMS devices the packaging and connection system is a main weak point, where e.g. cracks and delamination might occur due to thermo-mechanical stress, caused by CTE mismatches of the involved materials. Typical reliability test are therefore mostly performed by means of applying dedicated temperature profiles to the test samples, e.g. within a temperature / climate chamber. Chosen

temperature ranges are usually closely related to the later application scenario.

In case of the here described high temperature MEMS device, the intended operating temperature range reaches from -40 (or lower) up to 300°C, whereas for acceleration purposes even higher test temperatures might be required. State-of-the-art reliability test benches, such as temperature shock test chambers or climatic chambers, are typically covering only a temperature range up to 220°C, in few cases even a little bit more. However, temperature chambers for temperature ranges over room temperature can of course handle much higher temperatures (up to 2000°C and more), but as soon as lower temperatures (below 0°C) are required, the active cooling system, which is mostly based on vapor-compression refrigeration, faces strong problems with respect to the high temperatures (especially the refrigerants).

To overcome this current limitation, a new system for high-temperature reliability tests is currently in development and tailored to the specific requirements being defined by Fraunhofer ENAS. Its principle structure is shown in Fig 9.

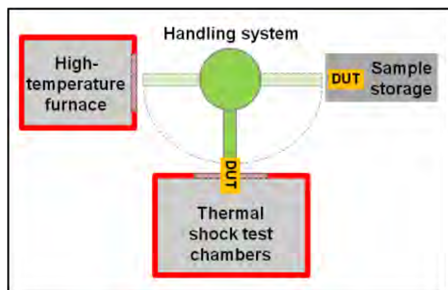

Fig. 9. Schematic drawing of the new developed high-temperature reliability test system for temperatures up to 450°C.

The basic idea is to use two individual temperature ovens with different temperature characteristics: a thermal shock test chamber system, specified for a temperature range between -70 and 220°C (cold chamber: -70…150°C, warm chamber: 50…250°C), and a high-temperature furnace for a temperature range between room temperature and up to 450°C. A handling system will be responsible for shifting the test samples between the different temperature chambers. That way, it becomes possible to perform reliability test over a wide temperature range from -70 to 450°C. For safety reasons, the test setup will be enclosed by a fence. The control of the test bench as well as the placement of the test samples (via a sample storage) will be done from outside. In addition, both furnaces can be used individually, to maximize the benefits of the system. However, one challenge can be seen in the adaption of an in-situ-measurements system, which is needed to monitor e.g. the resistance of daisy chain structures during reliability tests. Thus, further development work is required to be able to reliable determine the time-to-failure of the tested components.

Conclusion

In this work we demonstrate the initial steps to develop a packaging concept and a MEMS suitable for 300°C operation temperature. By combining heterogeneous materials a promising packaging concept will be realized either by thermo compression bonding or anodic bonding. The integration of TSVs and redistribution layers enable small device dimensions and low cost fabrication szenarios. Together reliability testing, physical failure analysis and numerical simulation establishes a design for reliability process that will accelerate the design and fabrication process.

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