

# A TIME-BASED CAPACITANCE TO DIGITAL CONVERTER WITH FAST DATA ACQUISITIONS AND HIGH RESOLUTION

Ali Heidary and Gerard C.M. Meijer

Electronic Instrumentation Laboratory, Delft University of Technology

Mekelweg 4, 2628 CD Delft, the Netherlands.

Phone +31 15 278 5026; Fax: +31 15 278 5755; E-mail: a.heidary@tudelft.nl

**Abstract:** This paper presents an integrated interface with a fast data-acquisition rate for capacitive sensor. Based on the results of an analysis of the Charge-Transfer Process, the maximum frequency, for which the systematic errors are still within a certain limit, has been calculated. It is shown how the noise of the applied relaxation oscillator can be reduced by using a pre-amplifier with the minimum required bandwidth in front of the comparator. Further improvement is obtained by reducing the noise of integrator current in the applied relaxation oscillator. The interface has been designed for implementation in  $0.7\mu\text{m}$  standard CMOS technology. Simulation results show that for a  $5\text{ pF}$  sensor capacitance with a parasitic capacitance of  $50\text{ pF}$  and a measurement time of  $100\text{ }\mu\text{s}$ , a resolution of 14 bits can be achieved while power consumption is less than  $5\text{ mW}$ .

## Introduction

Sometimes, in capacitive sensor applications, the bandwidth of the physical signals is low enough to improve the resolution by applying averaging of the output signal. In that case, a very high resolution can be achieved. However, in other cases, such as displacement measurement in a closed-loop system, in addition to a high resolution a high measurement speed is also needed. This can be achieved by a) decreasing the thermal noise by increasing the power consumption, b) applying low-noise circuit techniques and optimizing the noise behavior of the circuit, c) increasing the level of the drive signal.

In a high resolution displacement measurement, because of possible thermal expansion, very little power consumption is allowed at the position of the sensor head. Therefore, we should either keep the power consumption below a certain limit, or connect the sensor with a long cable to the interface. In the second approach we have to deal with a large parasitic capacitance of the connection cable. In this work we focus on reducing the power.

In earlier papers it has been shown, that the interface circuits can be designed based on the use of a capacitance-to-voltage converter and a relaxation oscillator, which offer the attractive features of simplicity and low-power consumption [1]. In this paper, we show how the noise performance of this interface circuit can be improved by using optimized low-noise circuit technique.

## The interface

Figure 1 shows the block diagram of the interface. As it can be seen, beside the unknown capacitor  $C_x$ , two reference capacitors  $C_{\text{ref1}}$  and  $C_{\text{ref2}}$  are also measured to perform three-signal auto-calibration [1, 2]. Each of these three capacitors is selected by the multiplexer. Next, in the front-end circuit, its value is converted to the voltage by a Capacitance-to-Voltage Converter (CVC). As a next step, the modifier converts the voltage to a period time.

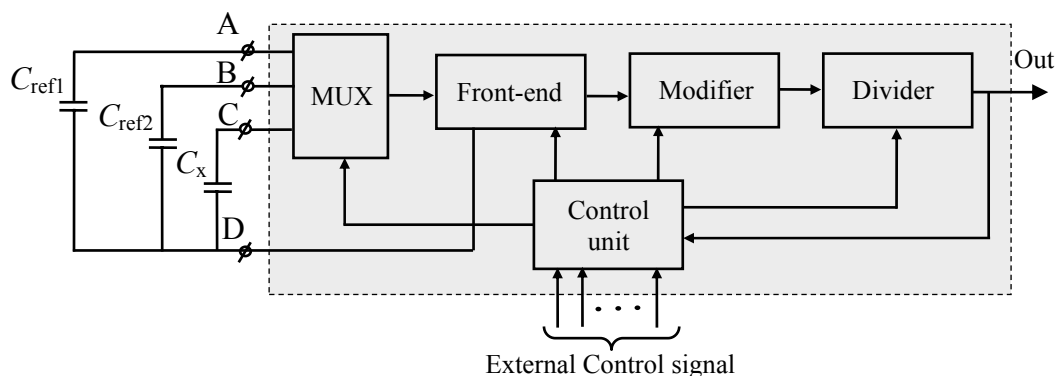


Figure 1: (a) The main structure of interface (b) the interface output signal.

Figure 2(a) shows the CVC for a floating capacitor [1, 2], while figure 2(b) shows some important signals. In order not to loss any charge, before transition in drive voltage,  $V_{drive}$ ,  $S_1$  is opened. In this CVC the drive voltage has two levels of 0 V and  $V_{dd}$ . When  $S_1$  is closed, phase 1, the drive voltage is sampled on  $C_x$ , and in phase 2 the charge of  $C_x V_{dd}$  is pumped in  $C_f$  which results a jump of  $V_x = C_x V_{dd} / C_f$  at the output.

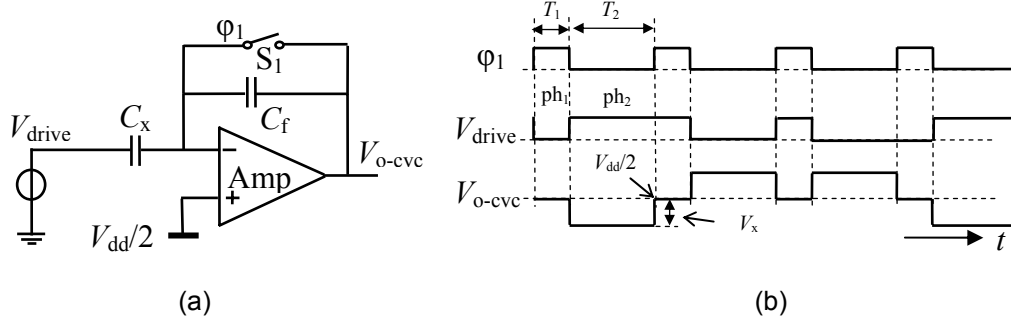


Figure 2: (a) The CVC for high-quality floating capacitor and (b) some important signals.

Figure 3(a) shows the voltage-to-period converter [1, 2] together with some important signals (Fig. 3(b)).

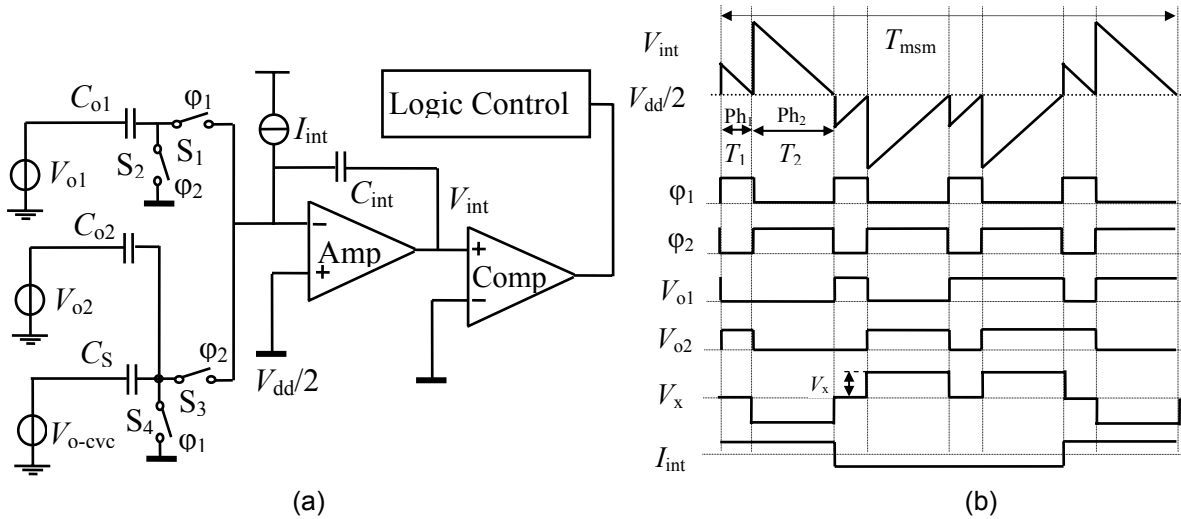


Figure 3: (a) The voltage to period converter and (b) some important signals.

The voltages  $V_{o1}$  and  $V_{o2}$  are block-shaped with the levels of 0 and  $V_{dd}$ . In phase 1 (Ph1), the charge  $Q_1 = V_{dd} C_{o1}$  of  $C_{o1}$  is pumped into the integrator capacitor. Next, this charge is removed by integration of  $I_{int}$ . In phase 2, the charge  $Q_2 = V_{dd} C_{o2} + V_{o-cvc} C_s$  is pumped into the integrator capacitor. This charge is also removed by integration of  $I_{int}$ . Therefore one complete measurement cycle,  $T_{msm}$ , amounts to:

$$T_{msm} = \frac{4(V_{dd}(C_{o1} + C_{o2}) + V_{o-cvc} C_s)}{I_{int}} \quad (1)$$

### Measurement speed

Since we want to have a fast measurement, the interface should run at a high frequency. In switched-capacitor circuit, the maximum frequency will be limited by the required accuracy [3]. If the system should have an  $N$ -bit performance, the settling error at the output must be less than half an LSB. This requires, the condition

$$e^{-T_2/\tau_{CT}} \leq 2^{N+1} \quad (2)$$

or equivalently

$$T_2 \geq (N+1)\tau_{CT} \ln 2 \quad (3)$$

to be satisfied, where  $\tau_{CT}$  is the charge-transfer time constant. Since  $T_2$  depends on input capacitance  $C_x$ , equation 3 should be valid for the minimum value of  $T_2$ , which is equal to  $T_1$ . Therefore, it should hold that

$$T_1 \geq (N+1)\tau_{CT} \ln 2 \quad (4)$$

Due to sensor and/or cable parasitic capacitances, the CVC will limit the upper-limit of the frequency. Our analysis shows, that using Opamp in the CVC is advantageous as compared to an OTA. Moreover it can be proven, that the charge-transfer time constant is proportional to  $C_p/C_{x,max}$ . Since this ratio is different in different application, in this design the frequency can be set by the user in 4 different values.

### Noise optimization

By increasing the measurement speed, if we do not increase the noise performance, the resolution will decrease. To increase the resolution, we did a noise analysis of the interface, which shows that in our interface the comparator and integrator current source are the two major sources of noise, as will be discussed now.

#### 1. Using a band-limited comparator instead of a standard comparator

A standard threshold-detecting comparator is usually designed as a wide-bandwidth high gain amplifier, possibly implemented with a cascade of low-gain amplifiers. Usually, the first stage of the cascaded amplifiers dominates the input-referred noise and sets the comparator noise bandwidth. To maximize the speed at a given power consumption, the capacitance at the output of the first stage is kept as small as possible, so that the input-referred noise of such an amplifier can be rather large [4]. It can be so large, that the noise performance of the interface is dominated by that of the comparator [5].

However, in our interface any delay-related error caused by comparator can be removed with the applied auto-calibration. Therefore, there is no need for a fast comparator. Therefore, instead of using a standard threshold comparator, a preamplifier with limited and controllable bandwidth followed by a Schmitt trigger is used (Fig. 4). The preamplifier has enough gain, so that the noise of the Schmitt trigger can be ignored. Using such a band-limited comparator will not only decrease its own noise contribution, but will also filter some part of the noise of the previous stages.

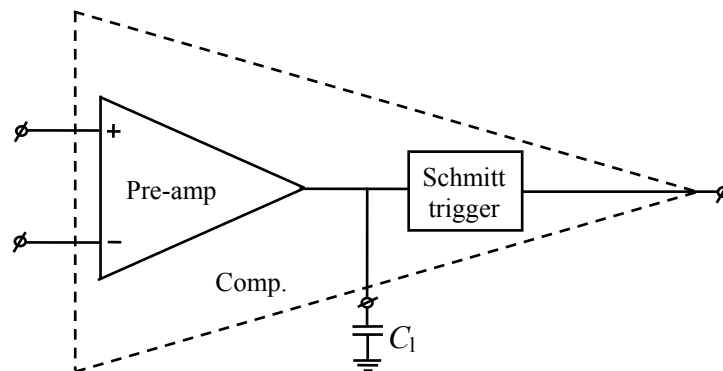


Figure 4: A comparator with limited and controllable bandwidth

#### 2. Decreasing the flicker noise of integrator current source

Our analysis shows that using a comparator with limited bandwidth has only little effect on the  $1/f$  noise contribution of the integrator current source Fig. 3(a). Therefore, in the new design, the noise of integrator current source can easily dominate in the total noise of the interface. Therefore the integrator current source is designed to have a flicker-noise-corner frequency of about 10 Hz. The remaining flicker noise can be removed by auto-calibration.

### Simulation results

The interface has been designed for implementation in 0.7 $\mu$ m standard CMOS technology. The simulation results show that with a power consumption of less than 5 mW (1mA at 5V) for a 5 pF sensor capacitor with parasitic capacitance of 50 pF, a resolution of 14 bit will be achieved within a measurement

time of 100  $\mu$ s (including auto-calibration). This figure of merit is about two bit better than that of previous versions of the same interface.

### **Conclusion**

The noise performance of an integrated interface for capacitive sensor has been optimized. The noise reduction has been achieved with two major changes in the original interface including: a) limitation of the comparator bandwidth and b) decreasing the flicker-noise-corner frequency of the integrator current source. The limitation of the measurement speed is analyzed and based on that an optimal oscillator frequency has been found. With all these changes a resolution of 14 bit is achieved within a measurement time of 100  $\mu$ s with a power consumption of less than 5 mW.

### **References**

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