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Challenges in Design and Development of Indigenous Flight Test Instrumentation System for a High Performance Fighter Aircraft

V Madhusudana Rao, Kishan Singh Chowhan, Vijay V Patel, NNSSRK Prasad and PS Subramanyam

Aeronautical Development Agency(ADA), PB No: 1718, Vimanapura Post, Bangalore-560 017,INDIA
Email: vmsrao@jetmail.ada.gov.in

ABSTRACT

Flight testing phase is a crucial phase of any aircraft development programme. Flight Test Instrumentation (FTI) is an important on-board subsystem to validate the design, assess the performance of all other subsystems at various in flight test conditions. It also plays major role in post flight data analysis and leads to obtain aircraft airworthiness certification. Development of flight test Instrumentation system for a high performance fighter aircraft is a challenging task. It demands high reliability to ensure safety apart from design constraints like compactness, light weight, large data handling, high data integrity features and conduction cooled design. FTI system with Open System Architecture provides significant advantages towards ease of maintenance, up gradation, technology insertion, obsolescence mitigation, etc.

This paper brings out FTI system with open system architecture and describes challenges faced in finalization of system architecture, selection of technologies, use of appropriate standards or processes for software development, evolving concepts and algorithms to improve system performance, realization of system hardware, test results, etc. Architecture optimization specific to certain requirements and prognosis of the system are discussed in brief. It also brings out challenges in realization of complex test rigs or facilities for functional and performance validation and Ground Support Equipment for ease of system configuration and analysis.

Key words: Flight Test Instrumentation (FTI), Fighter Aircraft, Open System Architecture (OSA), Reliability and Safety, VME and cPCI, Signal Conditioning and Data Acquisition (SCADA), High data integrity, Ground Support Equipments (GSE),Test Rigs, Architecture Optimization, and Prognosis.

1. INTRODUCTION

Modern fighter aircraft is a very complex platform. It integrates with a large number of state of art technology based subsystems. These sub systems are typically, quadruplex digital fly-by-wire flight control system, dual redundant full digital Avionics System with Glass cockpit, Computer control and monitoring of essential systems (Electrical, Hydraulic, Fuel, Nose wheel Steering, Brake management and Environmental Control systems), Highly integrated communication systems, High performance display systems, Advanced and highly integrated sensors, high performance Engine with Full Authority Digital Control(FADC), state of art weapon system, and light weight, high strength structures for better performance.

Flight testing of such a complex platform demands sophisticated Flight Test Instrumentation (FTI) system. There are few vendors internationally supplying qualified FTI system. Most of the fighter programmes procure and uses these commercially off the self FTI systems supplied by these vendors. Largely these commercially off the self systems are based on proprietary bus architecture and this imposes constraints on up gradation /modifications, technology insertion, long term maintenance, life cycle cost management, etc,. Hence there was a need for development of FTI system with *Open System Architecture* to overcome these constraints. This system has features like, easy to reconfigure, compact with high data integrity, have adequate data bandwidth for real time transmission, be sufficiently large capacity for on board storage and ease of post flight data analysis. As the flight testing spans over considerable periods, FTI system has capability for up gradation or technology insertion to mitigate components / subsystems obsolescence issues. System is modular to enable expansion based on flight test requirements. Data formats and standards adopted are compatible to external system interfaces for better compatibility and also for quick and user friendly data analysis.

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FTI system monitors (for real time transmission) and records (for On-board storage) data from flight critical systems like digital fly-by-wire flight Control System for aerodynamically unstable aircraft. Therefore, along with performance and functionality of FTI system, its reliability and data integrity should be adequately high. As the FTI system has to handle different types of voluminous data at high speeds, it needs adequately large computational power. In addition, IVHM also demands on line processing for some of aircraft parameters. Configuring, developing and qualifying a system with all these requirements is a challenge for FTI system designers.

The simple block diagram of an on-board FTI system is shown in Figure 1.

It shows typical various types of inputs to FTI system where tapped parameters are taken from existing sensors of a system. In general data acquisition from digital serial interface does not need any signal conditioning. Data processing block is computationally intensive and it has to segregate required data and format for real time transmission. In addition data needs to be formatted and stored onboard in real time which is used for post flight data analysis.

2.0 DESIGN CHALLENGES

The primary goal for FTI system is to monitor data for flight safety and performance. Vehicle complexity is one of the key drivers for the selection and application of FTI equipment. As the amount of vehicle data increases, the demands on the FTI system increase as well. The ability to efficiently handle large amounts of data results in a direct reduction in number of flight test hours [1]

The overall configuration of a FTI system is shown in Fig 2.

The key design challenges are 1. Architecture finalization, 2. Selection of technology options, 3. SCADA modules design finalization, 4. Scheduler design, 5. Design of formatting techniques/algorithms for large data processing including IVHM, 6. PCM encoder with digital pre-mod filter and additional serial output, 7. Design of system configuration file, 8. GSE design to support ground operations including maintenance, 9. Sensor/interface simulation rig design, 10. System level test rig design.

2.1 Architecture finalization: Arriving at an optimum architecture is an important part of a system design. The system architecture decides the overall reliability and performance [1] [6]. Commercially off the shelf FTI systems available are designed based on proprietary backplane bus. Common architecture for instrumentation Systems (CAIS) based FTI systems are being used on some of the fighter programmes [2]. In this development, the Open System Architecture (OSA) was considered for the FTI system design to take advantages of ease of upgradation, maintenance, obsolescence mitigation and technology insertion [3] [4].

Open System is a system that implements sufficient open specifications for interfaces, services, and supporting formats for wide range of systems with minimal changes, to interoperate with other components on local and remote systems.

Architecture is finalized with centralized processing and distributed acquisition nodes.

2.2 Selection of Technology options: Open System Architecture (OSA) based system design is supported by various buses. Some of these buses used for aerospace or commercial applications listed in Table-1. As part of technology development initiative, an Open Architecture based data acquisition and processing unit of the FTI

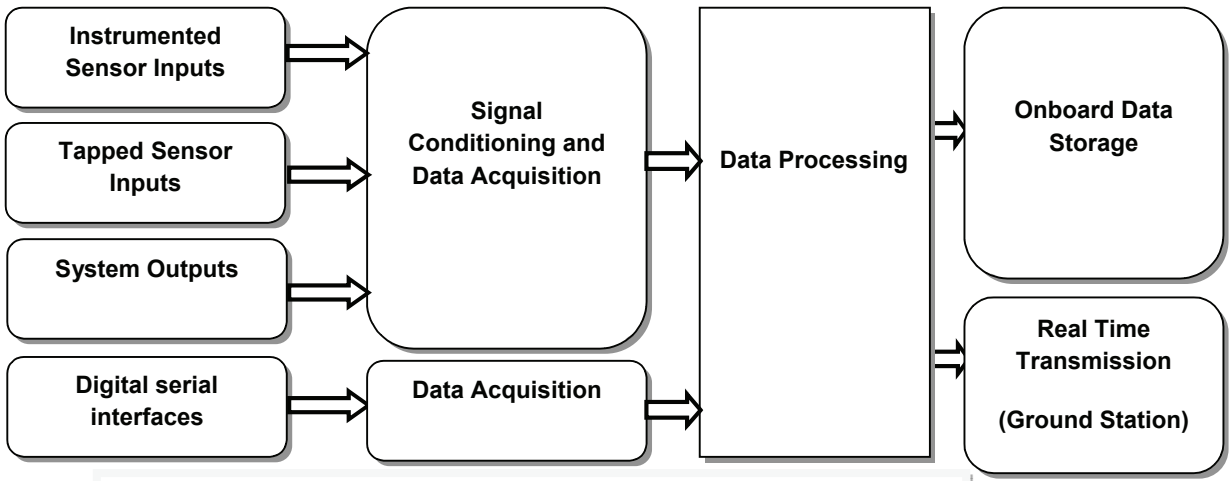

Fig-1: Block Schematic of an onboard Telemetry System

system was developed. Sensors were bought out items and other subsystems were already developed and in use. Making a decision on extent of usage of COTS items verses items/ hardware to be newly design and develop was a great challenge. This decision was made after assessing available technologies, feasibility of design, development time and mandated requirements. The quantum of effort required for development and risk mitigation were also considered for making decision.

2.3. SCADA modules design finalization: The modules are designed with cPCI bus interface. 13 different modules for 14 types of interfaces were designed and developed. The design challenges encountered for SCADA modules are: a) Handling of design complexity for significantly large number of channels per 3U cPCI form factor, b) Complex design process as large number of interface modules are being developed simultaneously, c) finalization of large variety of component sets for 13 different types of modules as all components are not available in required grade and temperature range. d) Selection of components with minimum foot prints to meet available floor area on the board. e) Finalization of field configurable parameters like gains, filters, input ranges, number of samples, etc., f) Finalization of device drivers functionality optimally, g) Finalization of test plans and procedures for all 14 types of interfaces.

2.4. Scheduler design: FTI system has to handle large number of IOs. These IOs are distributed over multiple remote acquisition nodes. The system architecture is optimized such that all IO signals are connected to Remote Acquisition Units (RAUs) and high speed serial buses like Mil-Std-1553B, RS422, etc are directly connected to DACENT.

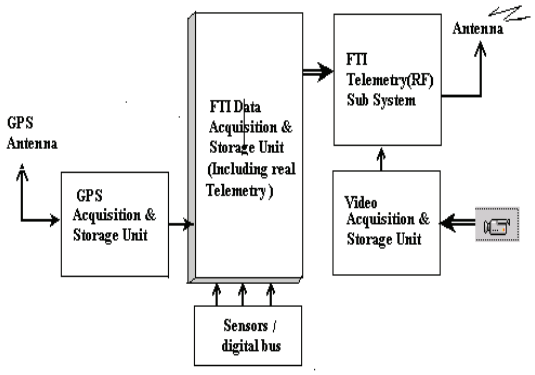

Fig 2: FTI system configuration.

Table-1 : Open System Buses for commercial and aerospace applications.

SL	TYPE	STANDARD	WIDTH(BITS)	RATE	APPLICATION
1	VME / VME64X	IEEE P1014 – 1987 (1981)	32/64	40/80Mbps	Avionics
2	cPCI	PCI SIG-2.1(1987)	32/64	132/264Mbps	Commercial /Avionics
3	PC104	IEEE P996.1 (1987)	8/16	8/16Mbps	Industrial/ Avionics
4	Futurebus+	IEEE 896.5a (1994)	32	100Mbps	Military
5	Mark33 (DIT)	ARINC 429 (1977)	25/32	100kbps/ 12.5kbps	Commercial Aircrafts

FTI system architecture is shown in fig-3. This topology and real time data transmission as per IRIG-106 was the base for scheduler design. The challenges in Scheduler design are: a) Design of sub minor frame sequencer for collecting data from remote acquisition nodes. b) Synchronizing minor frame data acquired with respect to minor frames (as per IRIG-106) in real time transmission. c) Finalizing scan sequence, scan command and data buffers based on required frame format. d) Designing separate data scan scheduler for real time transmission and on-board data storage, e) Time synchronization of various parameters acquired in different remote acquisition units.

2.5 Design of large data processing and formatting techniques/algorithms: To acquire and process large data in real time including on-line processing requirements of IVHM in DACENT, two high end processor modules were used in master and slave configuration. *Master processor module* is dedicated for handling system power-up sequence, Built-in tests, data acquisition on all interfaces. *Slave Processor module* is used for data collection from master module through shared memory, data processing, segregation of data for real time transmission as per configured minor frame format (IRIG-106 frame format), transmission of real time data through PCM encoder, formatting and storing of acquired data on-board as per customized IRIG -107 format. The challenges are: a) Finalizing real time large data transfer mechanism from master to slave module without data loss, b) Evolving techniques for selecting required data from various acquisition sources in real time for telemetry, c) Techniques for formatting data in

packet form for on-board storage, d) design of optimum data/write cycles for efficient storage of large data, e) Evolving hand shaking mechanism between slave processor and PCM encoder module and f) Handling of data for real time transmission.

2.6 PCM encoder with digital pre-mod filter and additional serial output: PMC based PCM Encoder with full functionality was designed and developed with digital pre-mod filter. Complete implementation was done in FPGA. Programmable digital pre-mod filter was implemented in FPGA with external DAC circuit. It is a unique implementation which eliminated programmable cut off analog filter components on the board. Dual buffer and handshaking mechanisms were implemented for taking the data from host processor without data loss. Another important feature of this module is implementation of RS422 serial interface data output along with PCM output. This interface can be enabled through a configuration file and baud rate can be programmed according to the Bit rate of PCM output. This technique simplifies the process of acquiring the data in-situ and processing while PCM output is connected to RF chain/transmitter.

2.7 Design of system configuration file: The concept of single point access for system configuration and maintenance has been adopted for FTI system towards ease of operation. Complete configuration file is generated for the system on ground using laptop/GSE and down loaded to FTI system through RS422 interface. Configuration file has all the information required to configure the system like selection of remote acquisition units, data acquisition modules, selection of channels, selection of gains, filters, input ranges, scan sequence for data collection from RAUs, initialization parameters of DACENT modules, number of minor frames in major frame, minor frame configuration (Synch width, Synch pattern, data width, number of data words, SFID type, time format, etc), PCM bit rate, data format details for real time transmission and on-board storage, etc.

2.8 GSE design to support all ground operations including maintenance: The design challenges are: a) Compact and portable design, b) complete configuration file generation, c) Downloading and analyzing BIT files, d) On-board data download and complete analysis (text and graphical) with engineering unit conversion. High end rugged laptop with the Ethernet interface and RS422 interface card along with necessary application software is used to meet above requirements.

2.9 Sensor/interface signal simulation rig design: The functional and performance testing is a part of SCADA modules development. Towards this requirement, a testing with complete sensor / interface signal capability (14 types of sensor outputs/ interface signals with large channel count of order of 1000) was designed and developed. Design challenges are: a) Design for very low signal simulation, b) Programmability for dynamic input changes, c) Large IO handling d) Extensive GUI application development, e) Validation of the test Rig simulated outputs.

2.10. System level Test Rig design: This test rig was designed to cater for testing of FTI system at complete system level, Unit level and also at module level in association with sensor/interface signal simulation rig. It also has capability to simulate any IO configuration of an LRU or set of LRUs during system level testing. It provides capability for configuring and simulating all aircraft digital buses (7 No. of Mil-Std-1553B buses and 16 channels of high speed RS422 interfaces) and discrete IOs for cockpit interface in addition to simulation of RS485 bus interfaces of remote acquisition units (up to 32 numbers) for real time transmission and on-board storage. It has capability for simulation of DACENT with command/response mode to collect data from real/ simulated RAUs, processing and formatting data for real time transmission through PCM Encoder module, on board storage on to hard disk for post test data analysis. This facility also has capability to simulate complete GSE functionality with PCM

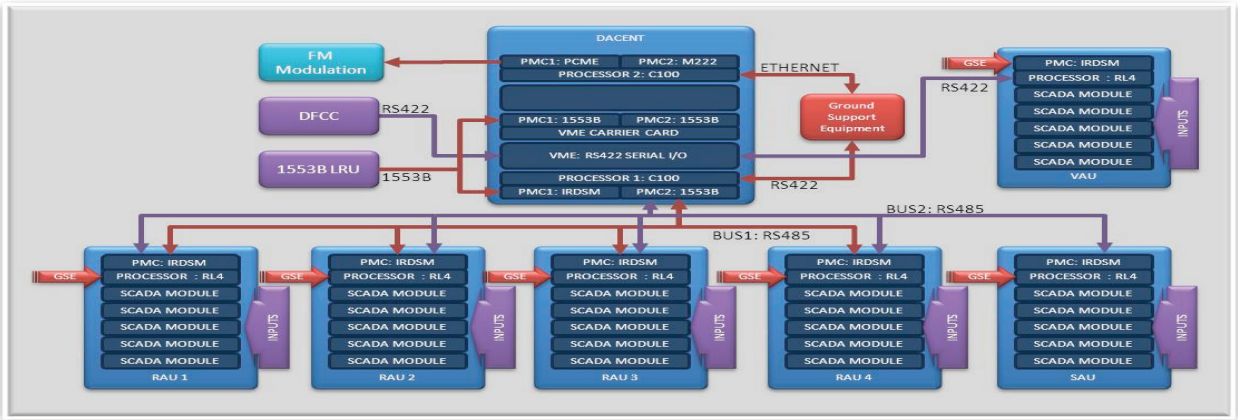

Fig-3: FTI System Architecture

decommutator and RS 422 interfaces. Design challenges are: a) Simulation of large number of aircraft interfaces, b) Simulation of functionality of DACENT and RAUs, c) Generation of required configuration file and use of configuration file for simulation of various sub-systems. d) Providing functionally of GSE with capability to acquire PCM data, down load on-board storage data and perform detailed data analysis with test report generation. e) Capability to carryout self test and assess the health of the system completely including identifying the faulty module.

3.0 REALIZATION CHALLENGES

For system hardware realization, a logical and clear line was drawn between procurement of COTS modules and new hardware development. The realization strategies are: a) All processor modules (required for various subsystems) where design, development, testing and proving efforts are large, were decided to be used from off the shelf items (COTS). b) For the on board hardware which is specific to the aircraft requirement/system configuration and where there are not many suppliers in the market to support in future, it was decided go for fresh development. In this category, all signal conditioning and data acquisition modules (14 types), Intelligent real time Scan Module, PMC based PCM encoder with RS422 interface, chassis for DACENT(Ref fig:4) and RAUs(Ref fig:5) etc, were launched for new development, c) Requirements were captured, software development standard and processes (OOAD with iterative model) were finalized for DACENT and RAUs (Ref Tab-2). The important embedded software development strategy adopted here for various RAUs is *table driven software approach* based on the configuration file, which provides flexibility to use on any RAU and reduces development time drastically. d) Portable and rugged GSE was configured using off the shelf rugged laptop and with two PCI modules (RS422 and PCM decommutator) and software was developed. e) Sensor/ interface signal simulation rig and system level test rigs were developed as per the standard process for testing complete FTI system on ground, also to diagnose quickly faulty system up to module level.

Tab. 2: FTI on-board Software Dev. Process

Sl No	Process Item	Selection
1	Process Standard	DOD-STD-2167A
2	Software life Cycle	Iterative
3	Operating system	VxWork®
4	Methodology	OOAD
5	Language	'C' with MISRA Guide lines
6	Tools	UML, Clear case®
® Their respective Trade marks		

The realization challenges are: a) Finalizing the hardware and software requirements considering all features and future requirements. b) Finalization of development process and standards for on-board hardware and software. c) Freezing of all interface definitions at early stage to enable hardware and software development to progress concurrently, d) Development of algorithms for IRIG-106 format generation, e) Identifying and addressing of hardware, software integration issues. f) Sub-system integration issues and their resolution, g) Realization of test rigs with large IO requirements and integration of various sub systems, h) Building self test features and validating them, i) Mitigation of manpower attrition (with proper documentation, periodic training and overlap responsibility) as development took significant time.

Fig 4: DACENT Chassis and Hardware

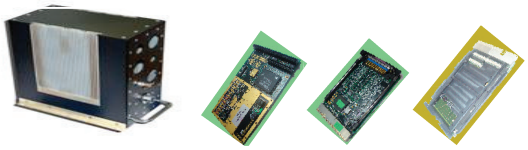

Fig 5: RAU Chassis and Hardware

4.0 ARCHITECTURE OPTIMIZATION

FTI System architecture has been optimized by design for a) Enhanced through put, b) In-situ reconfiguration, c) Ease of scalability, d) Ease of technology insertion, e) Extensive diagnosis coverage. These factors were considered right at initial concept studies and architecture evolution stage.

Enhanced through put is achieved through careful design of the architecture without any bottle necks for data transfer within the system and with the selection of high end processing modules as controllers at each node as well as for DACENT. *In-situ reconfiguration* is achieved with an architecture having single point access to the complete system through DACENT (DACENT in turn connected to all remote nodes on serial interface) using GSE. *Ease of scalability* is built in to the architecture by connecting DACENT with remote nodes using serial bus (RS485) which can be extended easily for 32 nodes. *Ease of technology insertion* is possible as Open System Architecture (OSA) has been deployed. *Extensive diagnosis coverage* was provided in the system as DACENT was connected to all remote nodes on serial bus (RS485) and it was easy to command and collect the diagnosis information for consolidation of overall system health status.

C-BIT (Continuous Built in test) is being carried out in each RAU and DACENT as a background process and these results are being transmitted to DACENT on minor frame scan. This has complete health information of RAU up to module level and even main blocks of acquisition path in a module. This data can be configured as a part of real time telemetry information to use for prognostic analysis on ground.

5.0 PERFORMANCE AND RESULTS

The FTI system performance figures are listed below in Table 3:

Tab.3: Performance comparison

Sl no	Parameter	Targeted system	Developed system	Relative Performance or figure
1	Throughput	20MBPS	40MBPS	Double
2	Channel Count	8	16	2 (Double)
3	On-board storage duration	2 H	3 Hours	Better
4	Up gradation / maintenance	Difficult	easy	Improved
5	Weight	Unit	less	lighter
6	Cost	Unit	less	Cost effective

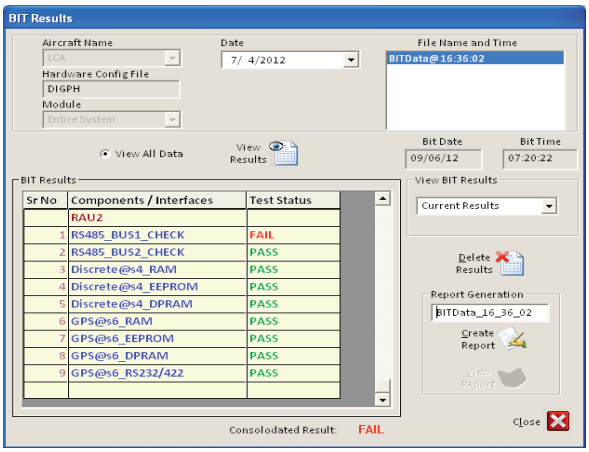

Fig 6: FTI System POST Results

The FTI System developed has been tested on Test Rig and test results like POST results (Ref fig:6), and telemetry data output in GUI screen(Ref fig: 7) are shown below.

Fig 7: Data from Real time Transmission

CONCLUSIONS

Challenges in design and development of FTI system for a high performance fighter aircraft are addressed in this paper.

The advantages of Open System Architecture (OSA) based FTI system over Commercially Off The shelf (COTS) systems available in the market with proprietary bus based architecture were discussed. Enhanced testability with additional RS422 interface on PCM Encoder also discussed in this paper. Process adopted for on-board Software development and testability features of the system like POST, BIT and CBIT also presented in this paper. Usage of CBIT results through real time telemetry for health monitoring and prognostic analysis also covered in this paper. Realization challenges for a complex and IO intensive FTI system are also brought in this paper. Optimization of an architecture for given set of functions is addressed. Complexity in realization of test rigs, levels of testing and test results are presented in this paper. Advance FTI system development with new technologies and with better performance is initiated for future programmes.

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