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Silicon Nanowire pH Sensors Fabricated Using Conventional CMOS Technologies

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Abstract:

This paper reports a fabrication method and an integration scheme for silicon nanowire (SNW) pH sensors. By using sidewall techniques, SNW with feature size down to nanometer regime can be obtained using conventional CMOS technology. The SNWs are operated in a FET configuration as a pH sensor, and sensitivity as high as 54.5 mV/pH for pH values from 1 to 12 is achieved.

Key words: silicon nanowire, CMOS, pH sensor, sidewall mask.

Introduction

Measurement of pH values are essential to chemical or biological applications such as environment and water quality monitoring, blood pH measurements, scientific research, DNA sequencing, and as many others [1]. A silicon nanowire (SNW) can measure pH values by operated in an ion-sensitive field effect transistor (ISFET). The carrier density of SNW channel is modulated through an electrostatic potential applied to the solution at the gate position. Because of the large surface-to-volume ratio of SNWs, high sensitivity has been achieved for SWN ISFETs in measurement of either pH or other biochemical targets [2].

One challenge for development of SNW sensors is that fabrication depends on patterning of tens or few hundreds of nano meter feature size. E-beam lithography is the most straightforward technique to fabricate nanowires [3], but the throughput and the cost are unsatisfactory. Advanced lithography such as extreme ultraviolet (EUV) is able to generate nanometer patterns with high throughput [4], but it is costly, inflexible, and hard for available. To solve this problem, this paper presents an approach to fabricate nanowires by using sidewall mask technology.

Sensor Fabrication

Fig. 1 shows the processes for fabrication of SNWs using sidewall mask technique. It starts with a silicon-on-insulator (SOI) wafer, which consists of a silicon device layer, a buried SiO_2 layer (BOX), and a substrate, see Fig. 1(a). A SiO_2 layer is deposited on the SOI wafer using plasma-enhanced chemical vapor deposition (PECVD), as shown in Fig. 1(b). The SiO_2 layer is patterned and etched using reactive ion etching (RIE), see Fig. 1(c).

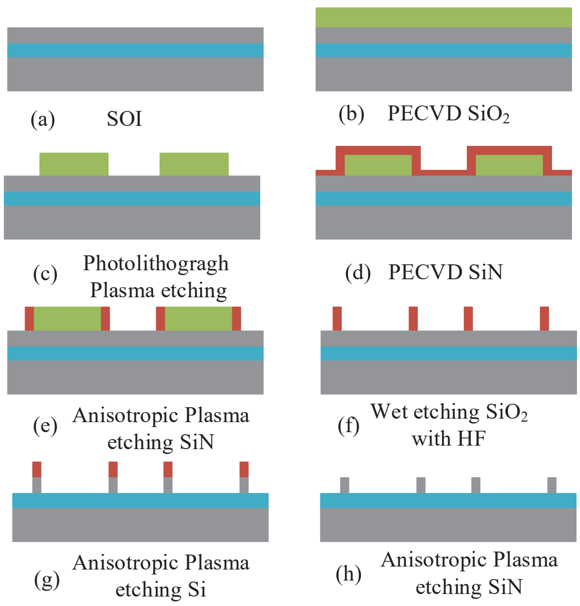

Fig. 1. Fabrication of silicon nanowires using sidewall technique.

A conformal SiN film with controlled thickness is deposited using PECVD, see Fig. 1(d), followed by anisotropic RIE etching to remove the SiN film on the wafer surface, see Fig. 1(e). Then the SiO_2 layer is removed using HF wet etching, after which the SiN film on the sidewalls of the SiO_2 patterns is left, see Fig. 1(f). Next the device layer of the SOI wafer is etched to form SNWs using RIE with the SiN patterns as the

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mask, see Fig. 1(g), followed by RIE etching to remove the SiN mask, see Fig. 1(h).

The SiN masks have a feature size determined by the thickness rather than photolithography. As the thickness can be controlled easily to tens or few hundreds nanometers using normal CMOS technology, it avoids usage of advanced and expensive lithography facilities.

SNW pH Sensors

Fig. 2 shows the as-fabricated SNW FET. The length of the SNW is 10 µm. The overall diameter of the nanowire is 350 nm, including a 150 nm SNW and a 100 nm silicon oxide insulator. Fig. 3 shows the scheme for flip-chip bonding of SNW with CMOS signal processing circuits, which are fabricated on separate wafers. For pH measurement, the gate voltage of the SNW FET is applied via a reference electrode immersed into the solution.

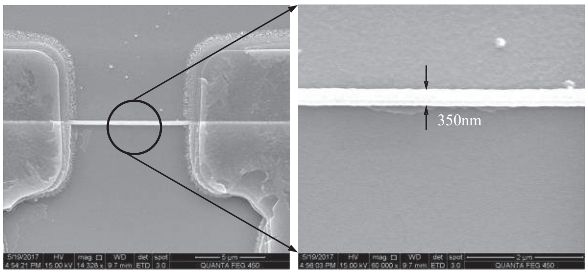

Fig. 2. Silicon nanowire sensor fabricated using sidewall technique.

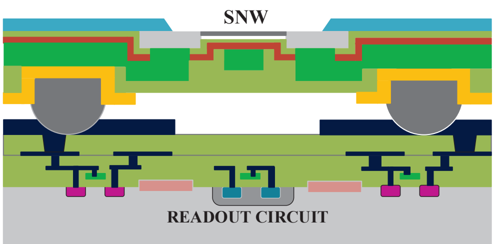

Fig. 3. Flip-chip integration of silicon nanowire with CMOS signal processing circuits.

Fig. 4(a) shows the drain current vs. drain voltages at pH values from 1 to 12 and constant gate solution voltage (Vg=-4V). The decrease in the absolute value of the threshold voltage causes increase in the drain-source current at a given gate voltage. Fig. 4 (b) shows the current vs. the gate voltage at pH values from 1 to 12 and constant drain voltage (Vd=-3 V). Since the SNW FET is P-type, the proton density at the interface decreases with the pH values of the gate solution, resulting in increases in the absolute value of the threshold voltage [4].

By using the drain currents, the thresholds to different pH values can be obtained, as shown in the inset in Fig. 4(b). Using the fitted line, the sensitivity of the SNW FET to pH values are calculated as 54.5 mV/pH. This sensitivity is slightly lower than the theoretical Nernstian value (59.5 mV/pH, 300K) [5], indicating that the SNW FET pH sensors fabricated using sidewall mask technology is highly sensitive.

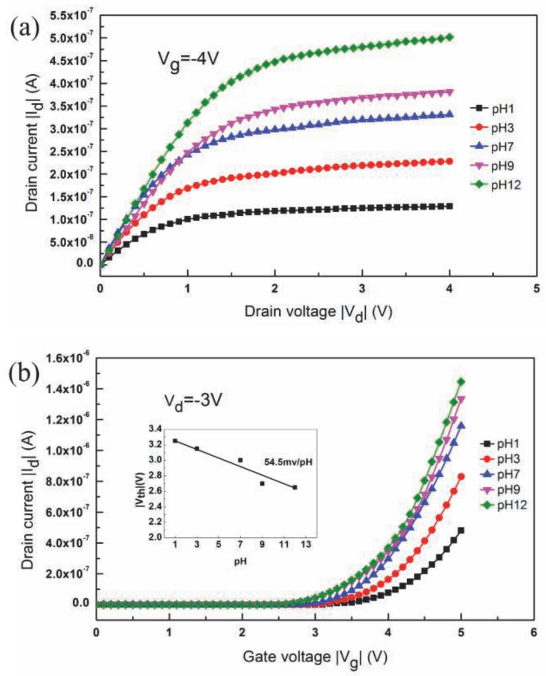

Fig. 4. The responses of the SNW FET vs different pH values. (a) Drain current vs. drain voltages. (b) The current vs. gate voltage.

Conclusion

A method for fabrication of silicon nanowires has been demonstrated. It can obtain tens or few hundreds nanometer feature sizes readily using the thickness of a thin film rather than advanced lithography facilities. This allows fabrication of SNWs with high output, low cost, and easy availability. The SNW pH sensor shows a high sensitivity of 54.5 mV/pH, close to the theoretical Nernstian limit of 59.5 mV/pH.

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