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Prediction and Compensation of Reference Voltage Shift in IC Sensors due to Mechanical Stress

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Abstract:
With the continuing miniaturization and integration of sensors challenges besides the scaling of the sensor itself arise especially for high precision measurements. Here the problem often lies in the growing impact of environmental influences compared to the smaller usable signals. In this talk the challenge of obtaining online high precision voltage measurements in the automotive environment using only ICs is discussed. The focus is set on the impact of mechanical stress on the reference voltage circuit needed to convert the analogue sensor signal into digital data. An approach of combining results of specialized measurement equipment to determine the expected use case specific stress influence with FEA and circuit simulations to develop a stress resilient on-chip voltage reference is presented.

Key words: automotive, mechanical stress, reference voltage, FEA and circuit simulation.

Introduction

In the growing field of electro mobility the use of lithium ion batteries is state of the art. This type of battery while providing good energy density is harder to manage than simpler lead based technologies. One challenge is the state-of-charge (SOC) determination as the maximum energy content changes considerably with age. Simple current integration does not take this effect into account. Another approach to determine SOC is measuring the cell voltage. However since small voltage changes correlate with large changes in charge this measurements must be very precise. While the required precision is easily obtainable using specialized measurement equipment the need for integration into the vehicle leads to other considerations. Measurements must be obtained and processed on a single battery-management-chip. In order for the ADC to convert the analogue signal into digital data which can be further processed a band-gap voltage reference circuit is used. This circuit is sensitive to environmental conditions such as temperature and mechanical stress. Since the former is already well compensated in state of the art components this work focuses on developing a concept for improving resilience to mechanical stress.

The approach calls for determining the expected stress levels and distribution in the use-case with specialized measurement-chips and FEA simulations, characterization of the stress dependent behavior of the components making up the band-gap-voltage-reference-circuit and developing ways to facilitate a stress resilient layout by modeling the circuits behavior under the determined stress.

Theory

At the core of the modeling done in this paper lies the change in electrical characteristics of silicon-based devices under mechanical stress. The physical effect is well modelled for bulk silicon as piezoresistive behavior following the equation [1]:

$$\frac{\Delta\rho}{\rho} = -\frac{\Delta\mu}{\mu} = \pi_{xx}\sigma_x + \pi_{xy}\sigma_y + \pi_{xz}\sigma_z \qquad (1)$$

With ρ being the electric resistivity, μ the carrier mobility and π_{xy} is the piezoresistive coefficient for the change in mobility in x-direction due to mechanical stress σ_y in y-direction. The effect of geometrical changes on the resistance is small compared to the effect of mobility change under mechanical stress and therefore disregarded.

For the behavior of devices e.g. transistors experimental determination of the change in drain current under mechanical stress shows great variances throughout the literature. Responsible for this are besides the varying levels of doping concentration the effects of other localized phenomena such as surface charge [2,3,4]. Since it is quite difficult to determine all variables influencing stress

dependence from the semiconductor fabrication process, and the link is sometimes not well understood, the change in current under mechanical stress will be determined directly for the devices used in the band-gap voltage reference so that a model specific to the devices in question can be developed.

Experimental Method

To extract the characteristic change in current due to stress wafer stripes are tested using the method of four-point-bending while electrical measurements are taken. Using this approach it is possible to determine the influence of the in-plane normal stresses (x- and y-direction). The size of out-of-plane stress (z-direction) in a packaged electronics setting is generally small in comparison to the in-plane stress and because the experimental setup for isolating it is complex it is not quantitatively considered. However some tests on the general occurrence of z-stress are performed to ensure that neglecting it is justified.

The four-point bending is performed on wafer stripes containing test circuits using a special bending apparatus. This device itself cannot determine the induced stress. It is therefore placed under a laser-scanning microscope, which is used to determine the bending radius of the wafer stripe. From this bending radius the strain ϵ on top of the stripe can be determined geometrically:

$$\epsilon = \frac{\Delta l}{l} = \frac{r_1}{r_0} - 1 = \frac{r_1}{r_1 - {}^{d}/_{2}} - 1 \qquad (3)$$

Where r_1 is the determined bending radius and r_0 is the radius without stress. While this is obviously infinite and therefore not usable it can also be understood as the radius to the neutral fiber in the center of the stripe which can be calculated as r_1 minus half of the thickness d of the stripe. Figure 1 shows the bending device being used with a PCB. For use with the wafer stripes an adapter was 3d-printed. The earlier approach of bending PCBs with the test chip on top was abandoned due to the resulting non constant bending radius and therefore stress across the chip.

From the determined strain the stress can be calculated via the elasticity of silicon (in the (100) plane, along the <110> direction Young's Modulus is E=169 GPa).

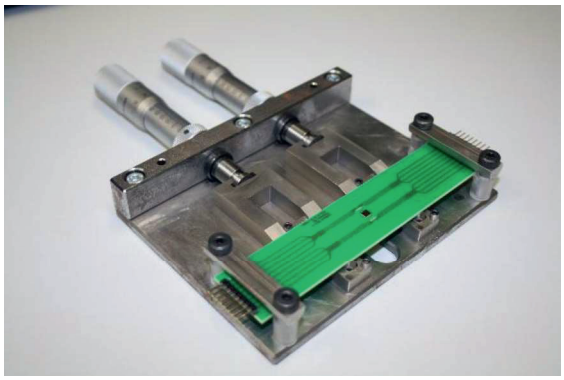

Fig. 1. The four-point-bending-apparatus.

The devices are tested electrically at constant voltages and the change in current at different stress levels is measured. The change due to variations in temperature of the device is then subtracted and a linear correlation between the remaining change in current and induced stress is derived. A typical result of the bending radius to current and strain to current correlation can be seen in Figure 2.

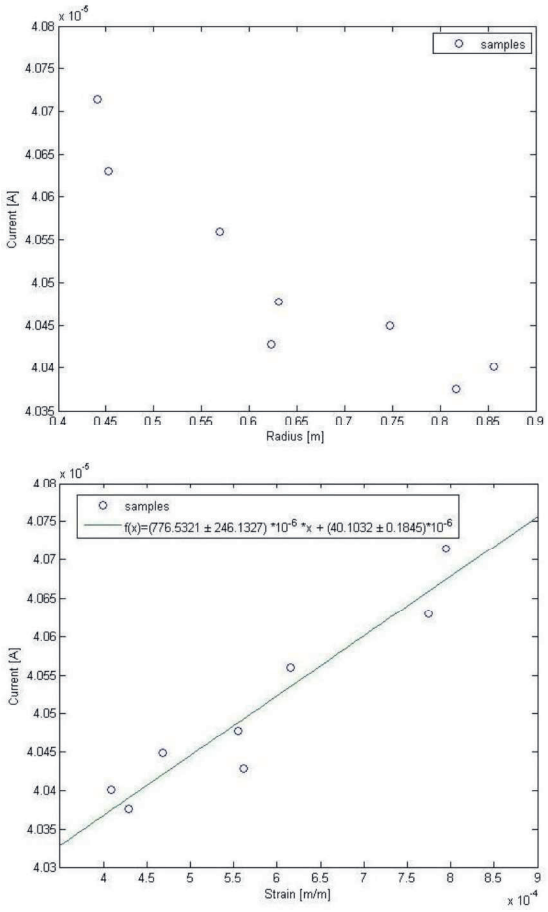

Fig. 2. Correlation between bending radius and current and strain and current

For application measurements a specialized stress measurement chip is used. This chip also uses the piezoresistive effect and matched current mirrors to determine the in-plane stress applied to it. It has been in continuous use since 2009 and the determined values are therefore seen as reliable. With it it's possible to determine relative in-plane stress meaning σ_x-σ_y with an accuracy of 5 MPa and the absolute value of σ_x or σ_y with an accuracy of 15 MPa. The measurements remain reliable with stress levels of up to 400 MPa and temperatures of 150 °C [5].

Device Model Validation

The results for the different tested devices are shown in Table 1 and compared to the values for bulk silicon.

Tab. 1: piezoresistive coefficients (|| indicating stress parallel to main current direction in the device,+ indicating orthogonal, the NPN Transistor has no predominant direction)

	$\frac{\Delta I}{I}$ measured [1/MPa]	$\frac{\Delta I}{I}$ bulk value [1/MPa]
pMOS ||	-0.14%	-0.07%
pMOS +	0.15%	0.07
nMOS ||	0.07%	0.04
nMOS +	0.04%	0.01
Res. ||	-0.20%	-0.07%
Res. +	0.05%	0.04%
NPN	-0.17%	-0.36%

To validate the characteristics the change in drain current is modeled into a spice simulation using current-controlled current sources. A small test circuit containing several of the devices is simulated under uniaxial in-plane stress. This circuit is then also measured using the same approach used for determining the individual device characteristics. The difference between simulated and measured values is determined to be no more than 10%.

Mechanical Stress in the Application

Taking measurements of the BMS in a moving vehicle was not possible. However measurements in the assembly process were obtained which can give some estimates for application stress since most of the mechanical stress actually comes from interaction between the BMS-Chip and its package.

Figure 3a shows the special stress distribution on the surface of one measurement chip inside a package induced by assembly (bonding, molding and soldering), while Figure 3b shows the mean and standard distribution of the stress in the lower right quarter of the chip.

As can be seen the stress in both x- and y-direction is greatest in the center (compression stress) and lowers considerably to the edges corresponding with the stress direction i.e. the stress in x-direction changes along the x-axis and the stress in y-direction along the y-axis while both remain constant along their orthogonal axis. It is interesting to note that while the stress is greatest in the center the stress gradient is lowest there. Therefore matching structures compensating for the stress by differentiating between two devices should be placed here, the higher absolute values notwithstanding, while non matched devices are best placed on the edge of the chip. Further it might be possible to find nearly gradient and in-plane stress difference free regions along the chip diagonals. However because of restrictions given by the need for efficient chip layout geometrically stretched compensational structures making use of these regions are not feasible.

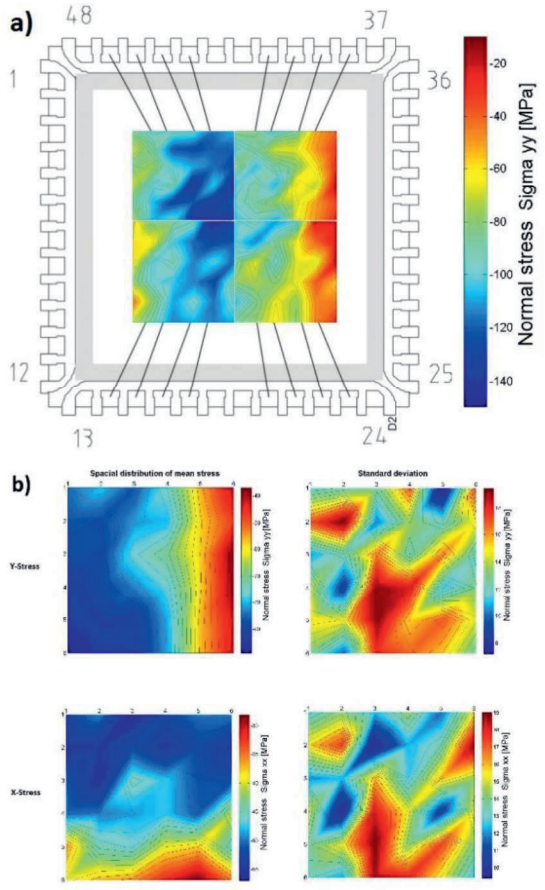

Fig. 3. a) The distribution of in-plane stress in the horizontal direction (y-Axis) in a single packaged chip is shown. b) mean and standard deviation chips) of the two normal in-plane stress components of the lower right quarter of 70 chips.

Out-of-plane stress

While the out-of-plane stress is supposed to be small in comparison to in-plane stress on the chip inside a package its effect was still investigated. For this purpose the stress measurement chip was indented at one of its measurement structures using a nano-indenter with a conical tip of 5 µm radius. It was determined that an indent made with 600 mN force destroyed the chips functionality while a force of less than 250 mN was not readable at the output of the measurement chip at all. The effect was highly localized only effecting the measurement structure directly indented with no carry over to its neighbors.

While no direct stress readings in the z-direction could be obtained it could still be concluded that no significant stress in z-direction was present in the application measurements. A stress in out-of-plane direction inside the package would have to come from contact with the molding material pressing down on the chip. Such a molding compound however consists in part of filling particles of which in a contact scenario some would stick out and press into the chip surface resulting in very high and highly localized out-of-plane stress. Since no such high variations of one individual test structure were found in all 70 test chips it was concluded that the no significant z-stress was induced.

Combining Simulations and Application Experiments

The simulation models are now used in combination with the application specific measurements to determine a stress optimized layout for the test circuit. For this purpose a simple program was written allowing to move around the devices or the test circuit as a whole on a map of the stress distribution over the chip. It also allowed to rotate the devices 90° individually. The approach closest to a real life application is moving the whole test circuit while keeping the devices close together i.e. not changing the size of the circuit layout but rotating the individual devices to obtain the best stress resistance. It could be shown that by manually testing circuit locations and device rotations the stress dependence of the whole test circuits $\Delta V/V$ could be variated by a factor of five (change between worst case and best case) thereby proving the concept of application specific stress resilient layout determination.

Conclusion

It could be shown that the method outlined in this paper is a workable approach for application specific mechanical stress resilient layout development. An improvement by a factor of fife could be shown for the relatively simple test circuit. It seems promising that for more complex designs and using more detailed models even greater improvements would be feasible.

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References

[1] A. A. Barlian et al., Review: Semiconductor Piezoresistance for Microsystems, Proc IEEE Inst Electr Electron Eng. 2009; 97(3): 513–552; doi: 10.1109/JPROC.2009.2013612

[2] R.C. Jaeger et al., CMOS stress sensors on [100] silicon, EEE Journal of Solid-State Circuits, Jan. 2000, Vol.35(1), pp.85-95; doi: 10.1109/4.818923

[3] K. Matsuda et al., Nonlinear piezoresistance effects in silicon, Journal of Applied Physics, 15 February 1993, Vol.73(4), pp.1838-1847; doi: 10.1063/1.353169

[4] R.C. Jaeger et al., Impact of mechanical stress on bipolar transistor current gain and Early voltage, 2013 IEEE SENSORS, Nov. 2013, pp.1-4; doi: 10.1109/ICSENS.2013.6688466

[5] H. Kittel et al., Abschlussbericht zum BMBF Verbundsvorhaben iForceSense, Bosch, 2008