

Universal Sensor Interface for High Performance Signal Processing Based on FPGA Technology

M. Selke, C. Nienhaus, D. Laumann, J. Doerr
 CANWAY TECHNOLOGY GMBH, Graf-Zeppelin-Ring 13, D-48346 Ostbevern
 mail@canway.de

Abstract:

Highly connected systems which are used in the scope of future manufacturing systems create huge challenges concerning their sensor interfaces and algorithms. The increasing complexity and growing data rates make it even more difficult to implement feature extractions close to the sensor. In order to fulfill these demands a powerful solution with the ability to react flexible to changing environmental conditions is needed. These characteristics are decisive features for a Field Programmable Gate Array (FPGA). FPGAs offer a highly flexible and powerful architecture to implement true parallel signal processing at high data rates in realtime. The present paper describes an approach to implement a modular and universal sensor interface using an FPGA to fulfill the various requirements of different sensor interfaces, algorithms and system connectivity. Besides the hardware and system description, this paper will demonstrate the use of different higher communication protocols in combination with software packages like LabVIEW. This extends the application of the sensor interface to algorithm evaluation e.g. in research and preliminary investigation.

Key words: Modular, High Speed, Realtime, Universal Sensor Interface, Measurement System.

This concept was developed as part of the BMBF funded project MoSeS-Pro, funding code 16ES0422.

Introduction

Today's industries have a growing demand for high speed, high resolution measurements, for example state recognition of manufacturing equipment to avoid early failures. This requires complex processing units like DSP or FPGA systems. These devices have plenty of characteristics that can cause problems in the development phase with effects on costs, risks and time to market. Frequently problems are caused by the complex power supply or difficult routing requirements for high speed memory devices. Solutions can be found in using versatile modules instead of application specific hardware implementations.

This essay illustrates a concept of FPGA based modules. These modules are specially designed to set up measurement systems. They can either be used standalone for small sensor applications or interact over bus infrastructure to build up complex systems.

In addition to using an FPGA as processing unit a Digital Signal Processor (DSP) can be chosen. A DSP is a processor which is optimized for digital signal processing. Compared to an FPGA common DSPs are

much cheaper. Their function scope is however restricted [1]. It is not possible to change peripheral interface topology. This means that in any case of overloading the resources of the DSP a new base board has to be developed.

A major aspect favoring an FPGA is the ability for true parallel processing. On the contrary the parallel processing capabilities of a DSP are limited. Moreover another task can however influence the previous one. Algorithm blocks in an FPGA are completely separated without influencing other parts of the logic. Another advantage of FPGAs is the easy achievement of true parallel sampling necessary for different algorithms.

FPGA Technology

To fulfill the requirements of a completely flexible hardware system, the usage of Field Programmable Gate Arrays (FPGAs) is currently the market leading technology. FPGAs are highly complex integrated digital circuits to adapt to many different applications. FPGAs are a further development of programmable logic devices. FPGAs contain a high amount of Programmable Logic Blocks (PLB) which perform complex combinational functions.

These PLBs are connected by reconfigurable interconnects to a total circuit. The configuration is described by a Hardware Description Language (HDL). Commonly VHDL or Verilog are used. HDL describes the behavior of the application and is used to compile a synthesizable digital circuit.

Most FPGAs also include memory blocks for storing data. They are often implemented as SRAM memory. The HDL is the same language which is used to produce an Application Specific Integrated Circuit (ASIC). ASICs are customized circuits that are designed for a particular application. Production costs are low, one-off costs however high. The function of an ASIC cannot be influenced in operation. Therefore FPGAs are often used to review the functionality beforehand.

FPGAs enable the possibility to evaluate a developed system and produce a concentrated circuit to realize the designated function of creating a sensor close measurement system. Modern chips combine an FPGA with embedded microprocessors as a System-on-a-Chip (SoC). This sophisticated technology allows performing serial and parallel data processing.

System Concept

The key component of the system is an FPGA device. As described earlier, FPGAs are highly modular and scalable devices with the ability of high speed and true parallel data processing. In contrast to microcontroller devices FPGAs are far more flexible concerning their interfacing possibilities. The interface is implemented by hardware primitives without need of special interfacing resources. This perfectly fits to a modular hardware concept. With the basic components described below, both small systems and high-performance measuring systems can be formed.

Basically, there are two different kinds of base boards: One board has an FPGA as processing unit. The other one has a SoC. Figure 1 shows the schematic representation of the FPGA base board.

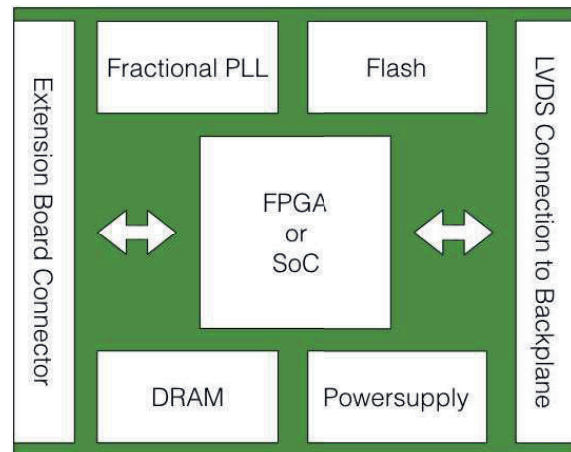


Fig. 1 FPGA / SoC Board, schematic representation

Beside the FPGA, there is a DRAM equipped. High density memory is often required for many complex algorithms. A connected Flash memory is holding the FPGA content. It may also be used to store specific configurations. The base board provides 64 inputs / outputs for an extension board. These input and output lines are length and impedance controlled. This is necessary for interacting with high speed data conversion circuits. A power supply with a wide input voltage range is provided. All necessary digital power rails are created on the board from one input voltage. An additional analog supply completely separated from the digital power rails can be fed in.

Another key component of the board is the high precision, multi output fractional Phase Lock Loop (PLL).

To be able to transfer a high amount of data to other connected components the backplane connections are accomplished as Low Voltage Differential Signals (LVDS). LVDS is an interface standard for high speed data transmission.

As a supplement to the FPGA board a SoC based board provides more opportunities for system building. Instead of an FPGA a SoC is the key component of this board. The SoC combines the performance of an ARM based hard processor with the flexibility of an FPGA. The processor enables the possibility to install an operating system on the module. Thus, the options for flexible and modular system building are extended. Besides the SoC the second base board is provided with the same basic components, a DRAM and a FLASH memory, 64 input / output lines and a backplane connection. Both base boards, FPGA and SoC, are equipped with a fractional PLL synthesizer. This component is able to create four different independent phase coherent output clocks. These clocks have a typical RMS jitter lower

than a few hundred femtoseconds with a wide output range from 100 Hz to 712.5 MHz. One example application for this clock generator is the generation of an analog to digital conversion strobe. The jitter of this strobe has fundamental performance influence on the signal to noise ratio. Equation 1 shows the relation between the Signal to Noise Ratio (SNR) and the jitter.

$$\text{SNR} = -20\log(2\pi \cdot f_{\text{in}} \cdot t_{\text{jitter}}) \quad (1)$$

It can easily be seen that the jitter has a direct influence on the SNR. Therefore a low jitter is important for high speed data conversion.

In addition to the base boards the system provides different extension boards. These boards represent the key feature of the modular concept. As there is no difference in the interface of both base boards, the extension board can be used either with the FPGA or the SoC base board, depending on system requirements. The extension boards can fulfill plenty of different needs.

Typical extension boards are analog to digital and digital to analog conversion boards with different resolutions, channel counts and speed grades. Digital interface boards to extend the possibilities of the base boards are also possible.

With this collection of extension boards and two different base boards numerous applications can be built up. If none of the existing extension boards fits into the desired application, a specialized extension will be less complex to redesign than the whole hardware because complex parts have already been placed on the base modules.

Figure 2 shows the first prototype from an early development phase. In this state, ADCs and the processing unit were grouped on one circuit board.

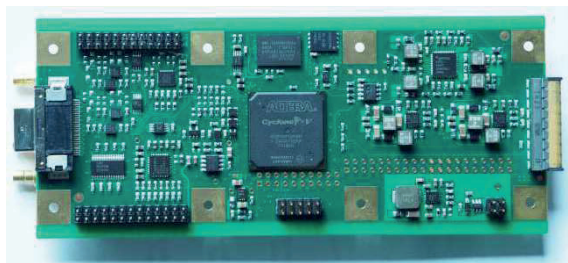


Fig. 2 First Prototype

Application

This concept can either be used as a high performance measurement system which is dynamically extensible or as a test system to evaluate algorithms.

In this section the modularity will be explained. For instance, if the vibration of a spindle axis test bench must be analyzed a 3D acceleration sensor will record the produced data. The sensor data are converted by three ADCs placed on the extension board. This board is connected to the FPGA board to analyze the captured sensor data. The calculated characteristics can be forwarded by UART, CAN or by any other communication interface (see Fig. 3). Also high level protocols like EtherCAT are possible. EtherCAT is a common protocol in the automation industry and is suitable for realtime requirements.

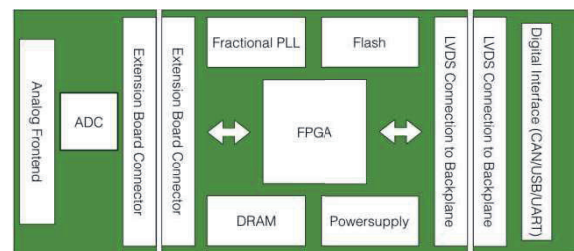


Fig. 3 Simple FPGA Configuration

While using a product additional demands may often occur. Sometimes these demands involve additional changes that cannot be implemented by current resources. If the application needs to provide the sensor data e.g. via a web interface an FPGA will not be presumed to be the best component. Therefore it is better to exchange the FPGA board by a SoC board (see Fig. 4). As SoCs are equipped with an ARM processor they are perfectly suited to run software tasks.

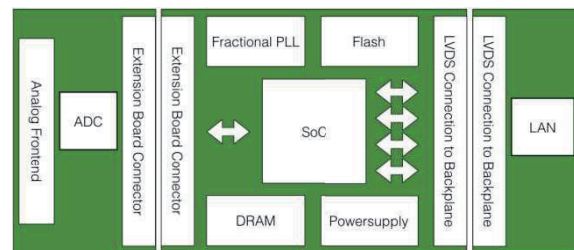


Fig. 4 Simple SoC Configuration

In a more complex design FPGA boards can be connected to a backplane linked to a SoC board combining incoming data. The maximum number of connected FPGA boards on the backplane is currently limited to four boards because the number of LVDS connections on the SOC board is restricted (see Fig. 5).

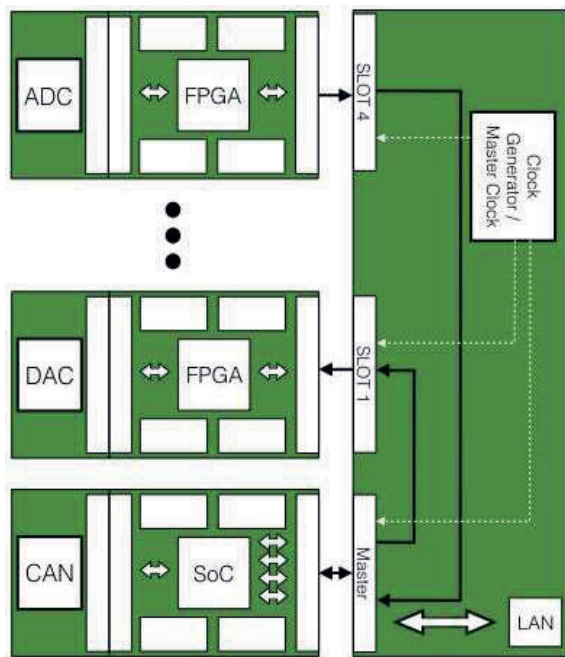


Fig. 5 Backplane Configuration

Using a SoC Linux can be applied to abstract the low level programming and create more complex applications. For further investigations the high amount of produced data can be streamed to a network server with the help of TCP. This also gives the possibility to use high level languages and tools (e.g. LabVIEW) to process and display the measured data. LabVIEW is a graphical program language from National Instruments¹. The software is able to create functional blocks for building up complex evaluation algorithms.

Potential fields of applications are the Internet of Things (IoT) or Industry 4.0 [3]. Especially Industry 4.0 demands solutions for conducting sensors and communication devices in order to improve production steps.

Advantages

Basically, the fundamental idea is to create a modular design in order to increase the reusability of the FPGA and SoC board. As a high amount of equal boards can be produced the costs per module will be reduced. If FPGA and SoC boards are successfully evaluated, simple extension boards will be developed more easily because of their minor complexity. Once all functions have been tested the whole design can be transferred to an ASIC. This step is useful if a high amount of the system is needed. All connected extension boards and the emerged ASIC can be combined on one PCB to produce a minimalistic design.

¹ <http://www.ni.com/labview>

SoC and FPGA board dimensions are almost as small as a common credit card (see Fig. 6). This form factor is well suited for many applications.

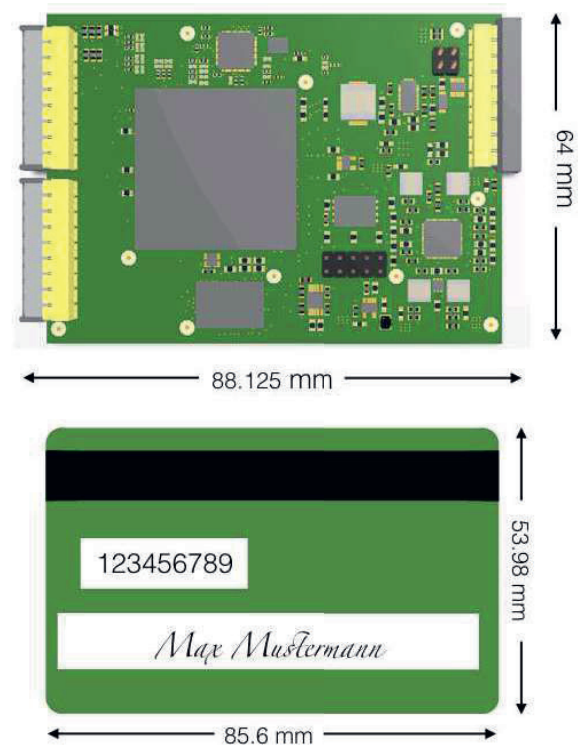


Fig. 6 Current FPGA Design

Software

In addition to the hardware described above, the concept of modularity is also implemented in the software and the FPGA code. Each extension board will have HDL components to interface the appropriate ADCs, DACs or other devices. This HDL block is an Intellectual Property core (IP-core). IP-cores are predefined function blocks that can be used to create chip designs. These IP-cores have standardized interfaces depending on the component group. An easy replacement of components to improve system behavior, costs and reliability without influencing the rest of the existing circuit has become possible (see Fig. 7).

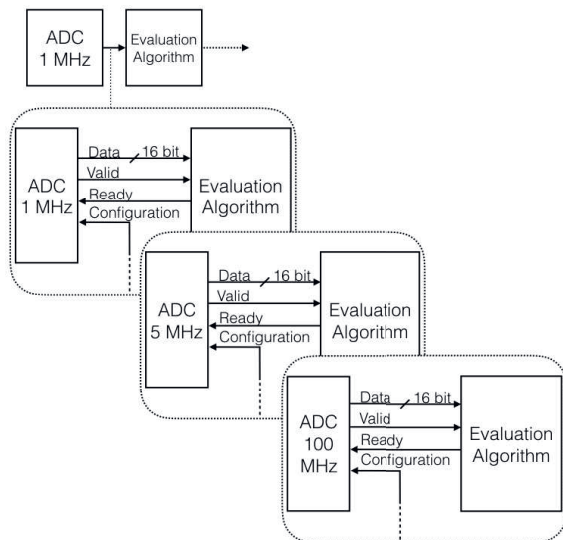


Fig. 7 ADC Interface

IP-Cores without a standard interface cause additional work on already tested algorithms and components in case of necessary exchanges. This could happen for instance when an extension board supplied with a 1 MHz ADC has to be replaced by a 5 MHz device. Every IP-core provides a standardized interface for internal FPGA communication so that a connection between various interface IP-cores and algorithms is possible. Each extension board has got its own ID so that connected extension boards can be verified.

Summary

The modular concept of FPGA, SoC and extension boards is a flexible solution for creating measurement or test systems. Compared to a DSP the FPGA technology has more advantages so that often even higher costs are justified. Parallel sampling and parallel processing is easy to achieve. The FPGA solution is the perfect processing unit because of its skill to implement nearly every algorithm and communication protocol. SoCs are the perfect complement to FPGAs for executing software tasks.

References

- [1] Berkeley Design Technology, Inc., Comparing FPGAs and DSPs for Embedded Signal Processing, http://www.bdti.com/MyBDTI/pubs/info_stanford02_fpgas.pdf, (2002) [Accessed: 13- Mar- 2017]
- [2] Linear Technology, Understanding the Effect of Clock Jitter on High Speed ADCs, <http://cds.linear.com/docs/en/design-note/dn1013f.pdf>, 2 (2013) [Accessed: 13- Mar- 2017]
- [3] PWC, Industry 4.0 – Opportunities and Challenges of the Industrial Internet, <https://i40-self-assessment.pwc.de/i40/study.pdf>, (2014) [Accessed: 20- Mar- 2017]

All product names, logos, and brands are property of their respective owners.