# RFID and Wireless Sensing

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**Abstract**

The efforts in realizing ubiquitous integrated circuits for ambient intelligence networks increased over the past few years. In particular, the passive radio frequency identification (RFID) presents a key technology for unattended wireless networks. A typical state of the art passive RFID system consists of an interrogator/reader and several passive Transponders. The interrogator communicates with the transponders by a wireless peer-to-peer connection and is responsible for the power supply of the passive transponders. To achieve a higher reading range and to improve the operational reliability of passive RFID sensor tags, the design of integrated circuits with an ultra low-power consumption and novel concepts for high-efficiency energy scavenging are required.

**Index Terms**: RFID, radio frequency identification, sensor networks, wireless sensing, ubiquitous networks, ADC

## 1 Introduction

Over the past few years, the application of the radio frequency identification (RFID) technology for the use in ubiquitous sensor networks gained a lot of interest and is nowadays a well known synonym for integrated low cost identification and sensor devices. Further, the strong social demand and customer needs to keep the security, reliability and product quality control on the more higher level is a reason for the use of RFID applications [1] [2].

In comparison with other wireless transceiver technologies the use of passive RFID transponder devices offers several advantages not only for economical reasons. The wireless transmission of power allows a flexible and ubiquitous use of small, low cost transponders for passive sensing networks. In order to achieve the requirements, the common energy-harvesting approach is based on the rectification of electromagnetic power and the use of ultra low-power design techniques. The use of ambient energy for power supply is called energy scavenging and there exist several promising concepts [3]. In the second section of this paper some technological aspects of the of the ultra low-power transponder design are presented. The third section deals with the fundamentals of the ultra low-power rectification, the ASK (amplitude shift keying) demodulation and the integrated backscatter modulator. Section 4 covers the ultra low-power design aspects of sensor data acquisition circuits.

## 2 Technology Aims

Because passive RFID transponder devices are high-volume products for mass applications, the use of a low-cost technology is essential. To obtain cheaper tags in the cent domain with more operational reliability, a lot of scientific work is in progress in the area of low cost technology development, e.g. polymer electronics [4].

However, typical state of the art RFID transponder devices, especially for UHF applications, are fabricated in bulk CMOS technologies. The advantages in comparison to other possible technologies are the low static power consumption, the relatively low production costs, the controllable yield and a possible high complexity. Furthermore, it is state of the technology to combine analogue and digital circuit blocks with a non-volatile-memory (NVM) like EEPROM and other novel techniques [5]. Poly EEPROM is the established technology for ultra low-cost RFID applications with only small memory arrays [6]. The used technologies for passive RFID transponders typically feature gate lengths of 0.12 µm. A further shrinkage is not reasonable, due to the unproportional increase of the static power consumption. Even in the recent process generation the leakage losses are not even longer negligible and therefore ultra low-power design techniques are absolutely required.

## 3 Challenging Issues of Passive RF Front-End Design

The RF front-end of integrated passive transponders represents one of the most complex analogue devices used in the wireless communication area. The reason therefore is that in passive RFID transponder devices non-linear and time-variant components are coupled in a single node. Because the implemented topology depends on the requirements

given by the specific application for an ultra low-power front-end design it's essential to know the behavior and the interaction of the non-linear devices and the application. In this section some general approaches for the design of power-efficient passive transponder front-ends are presented.

### 3.1 Ultra Low-Power Rectification

Fig. 1 shows a typical topology of a single ended voltage multiplier circuit for the use at low power RF levels. The functionality of this rectifying structure is based on simple non-linear devices like Schottky-, pn- or MOS-diodes [7]. RF power rectifiers are usually compared by the overall efficiency $(\eta_0)$. This figure of merit is defined by

$$\eta_0 = \frac{\text{DC output power}}{\text{incident RF power}} \cdot 100\%. \tag{1}$$

The threshold voltage at the low power domain of the used rectifying diodes leads to the problem of a high input impedance, even at the fundamental frequency [8]. To achieve a high RF-to-DC power conversion a rectifying device with a low threshold voltage is required. The output voltage of this single ended rectifier can be obtained with the following equation:

$$V_{DC} = K_N N(V_{RF} - V_{th,D}) \tag{2}$$

Where $V_{DC}$ is the output voltage, $V_{th,D}$ the forward voltage drop of the diode, $V_{RF}$ is the voltage of the input, $N$ is the number of stages and $K_N$ is a constant dependant on the number of stages. According to (2) a low $V_{th,D}$ value is desired in order to obtain a high value of $V_{DC}$ with minimum $V_{RF}$. Of course this equation characterizes the complex non-linear relation of the incident RF power to the DC output power only insufficiently, but the quintessence is right. For a high efficient rectifier design, devices with a low forward voltage drop are essential [7]. To achive this requirement Shottky diodes are used in most high-efficient front-end designs. These diodes have, beside the low forward voltage drop, a low series resistance and a low Schottky junction capacitance [9] [10].

As mentioned in section 2 the bulk CMOS technology is mostly used for RFID transponder designs. In a standard low-cost CMOS process Schottky diodes are often not available and therefore standard MOS devices have to be used. Because simple MOS diodes have a higher forward voltage drop the efficiency of such rectifiers is lower. In the area of high efficient rectifiers design with MOS devices for ultra low-cost RFID transponders the research activities are still ongoing.

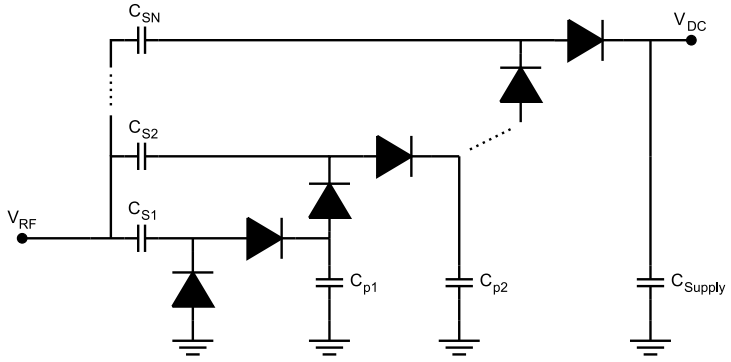


Figure 1: Single ended n-stage voltage multiplier (modified Dickson topology)

### 3.2 ASK Demodulator

The demodulator is an important block for a bi-directional RFID transponder. It recovers the information, which is ASK modulated on the carrier by the interrogator and delivers the data to the digital part. The demodulation technique is predetermined by the requirement for a low-power consumption of the demodulation circuit. A widely-used demodulation concept is the comparison of the carrier's envelope with the average value. The detection of the envelope signal can be implemented by using the same structure as that of the voltage multiplier with smaller number of stages. To receive the baseband data, a comparator compares the envelope and the low pass filtered envelope, which is the average value. Because voltage ripple from the envelope can interfere the data detection, the used comparator should have hysteresis [11] [12].

### 3.3 Backscatter Modulator

Backscattering of the incident RF power is the communication principle used in UHF RFID systems. It enables the tag-to-reader communication by varying the impedance of the RF node's analogue front-end in order to modulate the reflected power. There are two types of modulation allowed by EPC Global Gen2 standard for RFID backscattering communication [13]:

- Amplitude Shift Keying (ASK)
- Phase Shift Keying (PSK)

Both ASK and PSK modulate the complex impedance between two different states, but in a different way. The ASK modulation changes the real part of the impedance $Z_1 = R_1 + jX_1$, so the backscattered wave amplitude is modulated. PSK causes a change of the imaginary part of the impedance $Z_2 = R_2 + jX_2$ and thus a change in phase of the backscattered wave. As it is demonstrated in [12], [10] and [9] the ideal PSK modulation is more efficient than ASK because the available power to the tag is kept constant during both modulation states. But due to the fact, that several parasitic effects get more important at high frequencies common integrated backscatter modulators use a combination of PSK and ASK. The most reasonable modulation type depends on the available solid-state device technology. Figure 2 shows at the left side an implemented resistive ASK modulator and the modulator at the right is implemented by a time-variant capacitance (PSK).

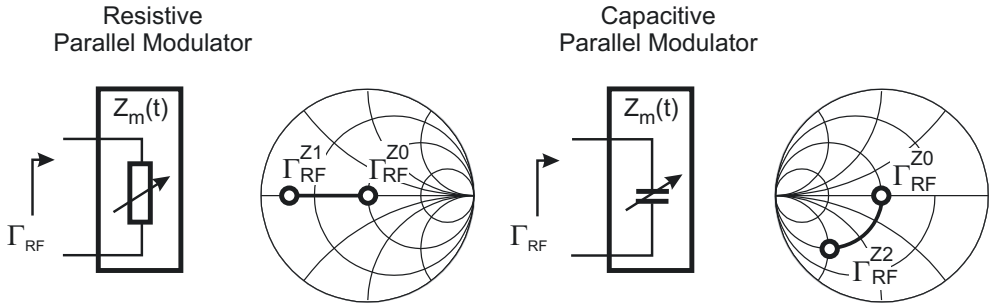


Figure 2: Passive backscatter modulator: Schematic topology and discrete smith-chart state representation

## 4 Data Acquisition

Acquiring sensor data for digital transfer in wireless networks can be achieved by different ways: direct conversion by means of circuit conditions and conversion by means of an analog to digital converter. A direct conversion of temperature to its digital representative is possible by making usage of the temperature coefficient of a circuit, e.g. an oscillator in [14]. If more than one physical dimension has to be converted by a wireless sensor node, a more general way of conversion with an ADC is needed. This section discusses the second possibility of using an ADC within a passive UHF RFID tag.

### 4.1 Analog to Digital Conversion for RFID Tags

Implementing an ADC for a passive wireless sensor node bears several challenges. Functionality needs to be ensured in a wide supply voltage range from 0.8 to 1.5 V, always with ripple on it. A high power supply rejection ratio (PSRR) is needed. The average current must not exceed 1 or 2 µA and high peak currents have to be avoided. This and the lack of fast oscillators imply, that ultra fast ADCs are barely possible within passive RFID tags. But ultra fast ADCs are not needed in RFID sensor systems, as the timing requirements are limited by the communication protocol used. UHF RFID systems commonly make use of the EPCglobal class1 gen2 UHF protocol [13]. This protocol specifies at highest link frequencies a timeout of 11.28 µs. This means an ADC with a conversion rate greater than 1/(11.28 µs) = 88.653 kSps is sufficient. A commonly used figure of merit (FOM) for making the energy efficiency of ADCs comparable to each other is defined by

$$FOM = P_{DC} \frac{1}{2^{ENOB} f_{sample}} \tag{3}$$

where $P_{DC}$ is the average power during conversion, $ENOB$ is the effective number of bits and $f_{sample}$ is the conversion rate. For an UHF RFID-integrated ADC typical values might be $P_{DC} = 1\,\mu W$, $ENOB = 7..8$ and $f_{sample} = 100\,kHz$.

Applying these values to (3) results in 78 fJ/conversion-step for ENOB = 7 and 39 fJ/conversion-step for ENOB = 8. As [15], [16] and [17] show, ultra low power ADCs were improved in recent years (illustrated in Fig. 3) making an implementation of an UHF RFID-integrated ADC conceivable. All presented solutions are successive approximation (SAR) type ADCs in slight variations and different technologies (all CMOS: 1.2 µm ,90 nm and 0.18 µm).

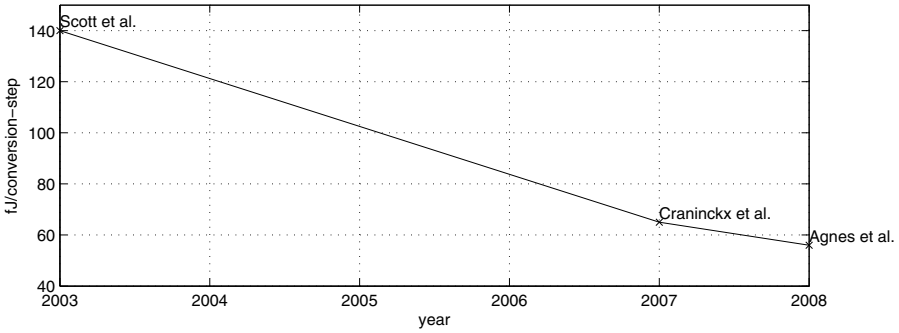


Figure 3: Ultra Low Power SAR ADC's figure of merit (FOM)

## 4.2 SAR ADC Architecture

Core elements of a SAR type ADC are a digital to analog converter (DAC), a successive approximation register and a comparator as illustrated in Fig. 4. The DAC is controlled by the successive approximation register and outputs an analog voltage based on a reference voltage $V_{ref\_pos}$ and the sampled input voltage $V_{in}$. The comparator digitizes the difference between $V_{ref\_pos}$ and DAC output voltage, which in turn controls the SAR's behavior. The register starts by setting the MSB. Depending on the input voltage $V_{in}$ being higher or lower than $V_{ref\_pos}/2$, the MSB is set back or stays. Continuing this procedure down to the LSB results in an n-Bit word, that could be read by a digital part of an RFID tag for serialization and backscattering.

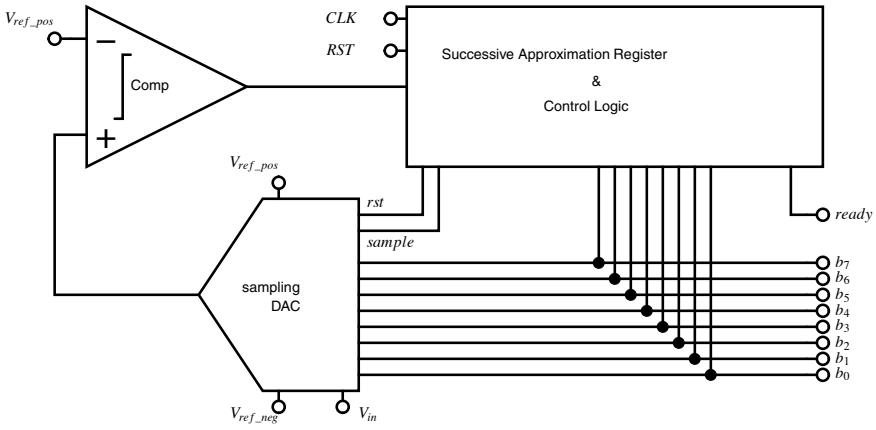


Figure 4: 8 Bit Successive Approximation ADC architecture with integrated sample & hold

## 4.3 Ultra Low-Power Techniques for SAR ADCs

Different methods transform the classical approach of the SAR architecture to a real ultra low power ADC. First there is the comparator consuming most of the current needed. This circuit is commonly implemented as a two stage differential amplifier. By clocking the bias current for one or both stages, the amount of quiescent current can be minimized. Another technique is bias clocking of the input stage and using a push-pull stage at the output. The latter method has the advantage of being very fast. But a designer has to be aware of too high peak currents. By replacing the classical comparator with a time domain implementation as presented in [17], another optimization might be reached. In this case a designer has to be aware of the time constant of the comparator circuit, which limits the applicable clock frequency.

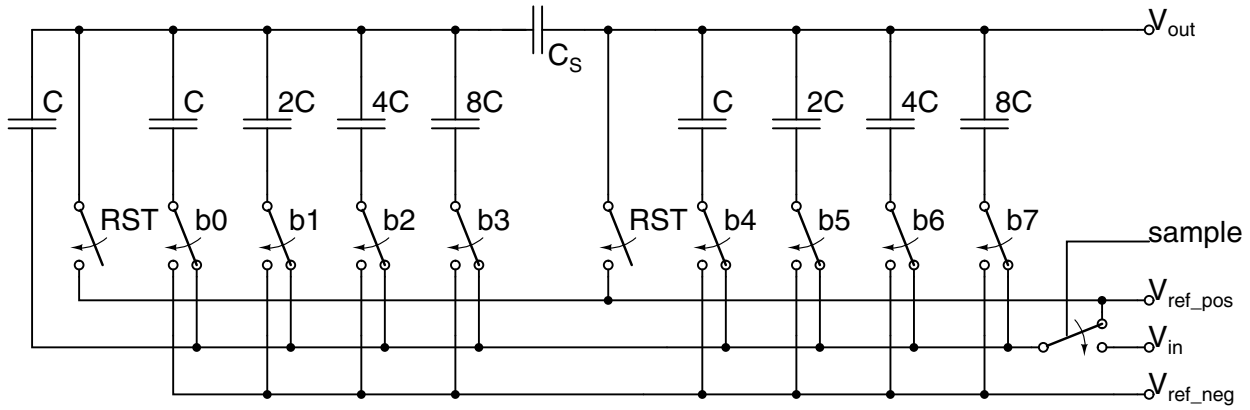


Figure 5: 8 Bit capacitive charge redistribution DAC consisting of two 4 Bit sub-DACs

Most DACs in SAR ADCs are designed by using the charge-redistribution technique first mentioned in [18]. Binary weighted capacitors are switched either to the positive reference voltage or to the negative reference voltage. The resolution of such DACs can be increased by combining two capacitive arrays with a scaling capacitor ($C_S$). An example is shown in Fig. 5, it consists of two sub-DACs, each with four Bit resolution.

This example circuit needs an inverted digital representative to generate the corresponding analog voltage (i.e. $V_{FSR} \Leftrightarrow 0x00$). During reset/sampling the top plates of all capacitors are pulled to the positive reference voltage $V_{ref\_pos}$ whereas the bottom plates' potential is $V_{in}$. When reset switches are opened and the sample switch goes back to $V_{ref\_pos}$, a charge of $Q = C_{all}(V_{ref\_pos} - V_{in})$ is conserved on the top plates. As the bottom plates' potential now is $V_{ref\_pos}$, the $V_{in}$-dependant offset potential on the top plates is $2V_{ref\_pos} - V_{in}$. The whole array works as a capacitive voltage divider. If any of the switches b0 to b7 are set to the negative reference voltage $V_{ref\_neg}$ (e.g. signal ground), the output voltage $V_{out}$ decreases by the corresponding voltage step. The successive approximation converges $V_{out}$ against $V_{ref\_pos}$.

What are the low energy aspects of this circuit? First, the integration of a sample and hold functionality into the DAC saves the energy needed for a dedicated sample and hold circuit. Second, the size of the capacitors can be minimized and thus save energy to charge them. A designer has to be aware of the accuracy of the binary weighted capacitors and particularly of the scaling capacitor. This one has to have a value of 16/15 $C_{unity}$ in the example of figure 5. In modern CMOS processes the unit capacity can have a value of down to several fF. Compared to a straight forward binary scaled 8 Bit DAC, the sub-DAC solution needs only 12.1 % of the capacitance.

The third component of a SAR ADC is the digital logic circuit containing the approximation register and some control signal generation. In modern CMOS processes different MOS transistor types are available. It is important to select the type with the lowest leakage current for the synthesis of the circuit. Choosing a type by speed issues can be neglected, as clock rates above several MHz will not occur within an UHF RFID.

## 5 Conclusion

Another promising approach to make RFID sensor nodes working more energy efficient is the usage of energy aware transmission protocols. In [19] a comparison between the TCP protocol and a new Simple Wireless Sensor Protocol (SWSP) is made. Although the SWSP is still demanding for wireless devices without a battery, this shows how protocols can be simplified saving more energy for the sensor itself instead for data transmission. Expanding the EPCglobal class1 gen2 UHF protocol [13] by some energy aware extensions for UHF RFID Sensor Tags can give significantly more power to RFID integrated sensors. Generally wireless sensing with passive RFID Tags can be summarized as a combination of several challenges. The energy harvesting from the electromagnetic field with the RF front-end not only has to supply a digital part, but also the sensor and data acquisition circuits. These circuits in turn have to be designed for fewest power consumption possible while featuring good PSRRs.

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